

Frank Hartmann

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Evolution of Silicon Sensor Technology in Particle Physics

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Evolution of Silicon Sensor Technology in Particle Physics

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Preface

In the post era of the Z and W discovery, after the observation of Jets at UA1 and UA2 at CERN, John Ellis visioned at a HEP conference at Lake Tahoe, California in 1983 “To proceed with high energy particle physics, one has to tag the flavour of the quarks!”

This statement reflects the need for a highly precise tracking device, being able to resolve secondary and tertiary vertices within high-particle densities. Since the distance between the primary interaction point and the secondary vertex is proportional to the lifetime of the participating particle, it is an excellent quantity to identify particle flavour in a very fast and precise way. In colliding beam experiments this method was applied especially to tag the presence of b quarks within particle jets. It was first introduced in the DELPHI experiment at LEP but soon followed by all collider experiments to date. The long expected t quark discovery was possible mainly with the help of the CDF silicon vertex tracker, providing the b quark information. In the beginning of the 21st century the new LHC experiments are beginning to take shape. CMS with its 206 m^2 of silicon area is perfectly suited to cope with the high luminosity environment. Even larger detectors are envisioned for the far future, like the SiLC project for the International Linear Collider. Silicon sensors matured from small 1 in. single-sided devices to large 6 in. double-sided, double metal detectors and to 6 in. single-sided radiation hard sensors. A large group of researchers inside the high energy physics community is steadily developing and investigating new devices and is pushing the technology to new limits. These larger and larger devices are the driving force to improve industrial processing and quality control. Also the readout electronics evolved from microsecond to nanosecond integration times and to radiation-tolerant sub-micron technology devices.

This review describes the successes in high energy physics as well as the developments in technology from the early days of NA11 to the current detector CMS at the LHC, ending with an outlook for detectors in a very early design phase for the future linear collider and the super-LHC. Also the day-to-day life in a silicon laboratory and the practical handling and testing strategies are described. Particle Physics examples will be given to underline the importance of silicon tracking devices for high energy physics.

August 2008

Karlsruhe,
Frank Hartmann

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I am especially grateful to Wim de Boer and Thomas Müller, Joe Incandela and Luigi Rolandi who supported me so much and who always had such confidence in me.

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Frank Hartmann

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Chapter 1

Basic Principles of a Silicon Detector

This introductory chapter introduces the basic silicon properties and their technical application to set the scene and provide understanding of the silicon sensors functionality. The writing concentrates on examples of detectors used in particle physics experiments – in the *High Energy Physics* (HEP). It also describes the working principle of silicon sensors as particle detectors, together with an explanation of their production processes, design parameter considerations and their reaction to radiation. A lot of teasers and links to information about detectors of the last and future 20 years are scattered in this chapter to underline the introduced parameters with real life examples. The examples are taken from *DE*tector with *Lepton*, *Photon* and *Hadron Identification* (DELPHI) (Chap. 3) at the former *Large Electron Positron* collider (*LEP*) at CERN in Geneva, the *Collider Detector at Fermilab* (*CDF*) residing at the *TEVATRON* collider at Fermilab near Chicago (Chap. 4), the *Compact Muon Solenoid* (*CMS*) experiment (Chap. 5) at the *Large Hadron Collider* (LHC) at CERN and finally the conceptual design considerations for the detectors at the future *International Linear Collider* (*ILC*). The chapter also briefly introduces silicon non-strip sensors. It concludes with a quality assurance description and a walk through prominent historic sensor failures.

1.1 Fundamental Silicon Properties

The Bible teaches us “In the beginning God created heaven and earth”. Today, we still do not know for sure what heaven is made of, but earth consists of, at least the upper crust, silicon and oxygen with some dirt (in the form of the other 90 elements) thrown in for added value.

Silicon, the element which revolutionized the development of electronics, is known as an important and multi-useable material, dominating today’s electronic technology. Its properties have been deeply investigated and are well known. Silicon is used in solar cells, computers and telecommunication systems. Initially silicon comes from the Latin word *silex*; *silicis*, meaning “flint”. The physical properties of silicon can be described as a hard, dark-grey solid with a bluish tinge. At ordinary temperatures, silicon is impervious to air. At high temperatures, silicon

reacts with oxygen, forming an inert layer of silica. Silicon is important in plant and animal life. Diatoms in both fresh and salt water extract silica from the water to use as a component of their cell walls. Silicon does not occur in the free, elemental state, but is found in the form of silicon dioxide and complex silicates. Jöns Jacob Berzelius is generally credited with the discovery of silicon in 1824. Deville prepared crystalline silicon in 1854, a second allotropic form of the element. Silicon is a semiconductor and a solid matter, which isolates at low temperatures and shows a measurable conductance at higher temperatures. The specific conductance of 10^2 to $10^{-9} \Omega^{-1} \text{cm}^{-1}$ lies somewhere between metals and insulators. Since the development of quantum mechanics the electrical conductance can be explained with the covalent bond in the crystal lattice. Bound electrons can be excited by inducing energy above threshold energy (gap energy), e.g. energy from light, x-ray, β -particles. Since the 1960s semiconductors have been used as particle detectors. Initially, they were operated in fixed-target experiments as calorimeters and as detectors with a high-precision track reconstruction. Since the late 1980s they have been widely used in collider experiments as silicon microstrip or silicon pixel detectors near the primary vertex. Silicon sensors have a very good intrinsic energy resolution: for every 3.6 eV released by a particle crossing the medium, one electron-hole pair is produced. Compared to about 30 eV required to ionize a gas molecule in a gaseous detector, one gets 10 times the number of particles in silicon. The average energy loss and high ionized particle number with $390 \text{ eV}/\mu\text{m} \sim 108 \text{ (electron-hole pairs)}/\mu\text{m}$ is effectively high due to the high density of silicon.

The usefulness and success of silicon can be explained in a handful of keywords:

- existence in abundance
- energy band gap
- possibility to change gap properties by defined adding of certain impurity atoms (dopants)
- the existence of a natural oxide

Since these topics are very exhaustively discussed in standard literature like [101, 137, 144], this book keeps the discussion on basic silicon properties, such as band gap, doping and *pn*-junctions brief. On the other hand concepts and formulas necessary for the understanding of the sensor functionality are presented as well as an overview of “standard” sensor designs and the reasons for certain ranges of parameters.

1.1.1 Just Silicon and Some Impurities

Quantitative properties of silicon are shown in Table 1.1. Silicon, as every semiconductor, has a forbidden region in the energy band structure, the band gap. At low temperature and in the absence of impurities (“intrinsic silicon”) the valence band is full and the conduction band is empty. Without any impurities, the concentration

Table 1.1 Silicon properties

Parameter	Symbol	Unit	Value
Atomic number			14
Relative atomic weight			28.0855
Structure			diamond
Lattice constant	a_0	Å	5.4307
Lattice orientation			$\langle 111 \rangle$
Electron configuration:			$1s^2 2s^2 2p^6 3s^2 3p^2$
Density	ρ	gcm^{-3}	2.328
Melting point	T_m	$^{\circ}\text{C}$	1414
Boiling point	T_b	$^{\circ}\text{C}$	2355
Gap energy (300 K)/(0 K)	E_g	eV	(1.124)/(1.170)
Dielectric constant	ϵ_r		11.7
Intrinsic carrier density	n_i	cm^{-3}	1.45×10^{-10}
Mobility			
– of the electrons	μ_e	$\text{cm}^2 [\text{Vs}]^{-1}$	1350
– of the holes	μ_h	$\text{cm}^2 [\text{Vs}]^{-1}$	450
Effective density of states			
– of the conductance band	N_c	cm^{-3}	3.22×10^{19}
– of the valence band	N_v	cm^{-3}	1.83×10^{19}
Max. electrical field	E_{max}	$\text{V}\mu\text{m}^{-1}$	30
Thermal expansion coefficient		$1/^{\circ}\text{C}$	2.5×10^{-6}
Intrinsic resistivity		$\text{k}\Omega \text{ cm}$	235

of electrons n in the conduction band and holes¹ p in the valence band are equal to the intrinsic concentration $n_i = n = p$. This is also reflected in the global charge neutrality at equilibrium. The mechanism to alter conductivity behaviour is to insert additional states in the forbidden region to increase the probability to excite electrons or holes in the Fermi–Dirac sense (see Fig. 1.1). The technical expression is called “doping”.

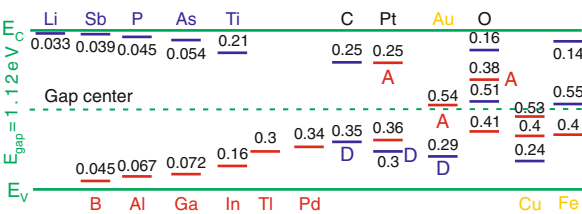


Fig. 1.1 The numerous impurities establish additional levels in the forbidden zone, e.g. boron near the valence band decreases the energy needed for hole excitation from 1.12 to 0.046 eV. Useful dopants add levels near the conduction or valence band. The A stands for acceptor, the D for donor. The levels introduced in the mid-gap region such as those from gold or copper are undesired and only increase leakage current but are not useful as attributed dopants

¹ Concept of “holes”: if an electron absorbs $E \geq \Delta E_{Gap}$ it can enter the conduction band leaving a vacancy called “hole” representing a positive charge in the valence band which can move in an applied electrical field. These holes are treated like particles and follow the Fermi–Dirac statistic.

Silicon is a type IV material (four valence electrons), it can be doped with impurities to alter its charge. One can produce “*n*-type” silicon by adding type V material, i.e. phosphorus (donor impurity; excess of electrons charge carriers; electrons as majority charge carriers); “*p*-type” material can be realized by adding type III material, i.e. boron (acceptor impurities; excess of holes as majority charge carriers).

Typical concentration levels are

- Si atoms $5 \times 10^{22} \text{ cm}^{-3}$
- $n_i = 1.45 \times 10^{10} \text{ cm}^{-3}$ at 27°C
- HEP silicon sensor *n*-bulk 10^{12} cm^{-3}
- HEP strip/pixel implant doping 10^{14} – 10^{16} cm^{-3}
- light doping (IC industry) 10^{16} cm^{-3}
- heavy doping (IC industry) 10^{19} cm^{-3}

In thermal equilibrium the probability for occupancy of one state at the energy E for the temperature T is given – taking into account the Pauli principle – by the Fermi–Dirac statistics

$$f(E, T) = \frac{1}{e^{(E-E_F)/kT} + 1} \quad (1.1)$$

where k is the Boltzmann constant and E_F the Fermi energy² or Fermi level.

$$f(E = E_F) = \frac{1}{2} \quad (1.2)$$

E_F can be regarded as the energy where exactly half of the available levels are occupied. With this knowledge, the location in the middle of the band gap for intrinsic silicon and in between the additional levels and the nearest band becomes obvious (see Fig. 1.1). The important point to remember is that the Fermi level is shifted depending on the impurities. The actual value of E_F level is essential, whenever a contact of two materials exists, because it defines naturally the relative levels of all the other bands (see Fig. 1.4).

In thermal equilibrium, the Fermi energy is constant everywhere.

The final number of free charge carriers is calculated as

$$n = \int_0^\infty D(E) \cdot f(E, T) \cdot dE \quad (1.3)$$

with $D(E)$ as the density of states, a pure quantum mechanical distribution counting all possible energy levels up to the energy E .

The technologically important point is that for all practical temperatures, the majority charge carrier concentration is identical to the dopant concentration, visible in the location of the corresponding E_F (see Fig. 1.1). The densities of electrons n and holes p then derive to

² Fermi energy: “the highest possible energy of a fermion at $T = 0 \text{ K}$ ”.

$$n = N_C e^{-\frac{E_C - E_F}{kT}} \text{ with } N_C = 2 \left(\frac{2\pi m_e^* kT}{h^2} \right)^{\frac{3}{2}} \quad (1.4)$$

and

$$p = N_V e^{-\frac{E_F - E_V}{kT}} \text{ with } N_V = 2 \left(\frac{2\pi m_h^* kT}{h^2} \right)^{\frac{3}{2}} \quad (1.5)$$

with N_C for conduction band and N_V as effective state density in the valence band. E_C , E_F and E_V are the energies of the conduction band, Fermi level and valence band. The m_e^* and m_h^* stand for the effective masses of electrons and holes, respectively, h is the Planck constant and the factor 2 is derived from the two possible spin states of the electrons. Obviously the charge neutrality still holds, but free electrons find their hole counterpart in the additional doping levels and no longer in the lower valence band. The famous mass action law holds for intrinsic as well as doped material:

$$n \cdot p = n_i^2 = N_C \cdot N_V e^{-\frac{E_g}{kT}} \quad (1.6)$$

where $E_g = E_C - E_V$.

To finally understand the electrical conduction mechanism, one has to know about mobility μ and drift velocity $v_D = \mu E$. It is not difficult to convince oneself that conduction depends on the number of free charges, their ability to move and their “motivation” to move. Translating this into a mathematical formula, the conductivity σ of doped silicon material comes to

$$\sigma = e(\mu_e n + \mu_h p) \text{ and therefore } \rho = \frac{1}{e(\mu_e n + \mu_h p)} \quad (1.7)$$

where e is the electron charge, μ_e and μ_h are the mobilities of electrons and holes, respectively, with mobility $\mu = \frac{v_D}{E}$ (E the electrical field, v_D the drift velocity), n and p are the densities of electrons and holes, respectively. Microscopically μ is given by

$$\mu_{e,h} = \frac{e\tau_s}{m_{e,h}^*} \quad (1.8)$$

and τ_s the time between scattering processes where scattering happens

1. at crystal defects, like dislocations or undesired impurities-this effect is not dominant before irradiation, but is the dominant part after
2. at intentionally introduced impurities, namely the doping atoms
3. at phonons, the thermally stimulated lattice vibrations

Since the mobility μ drops with increasing dopant concentration, the conductivity σ does not increase linearly with doping concentration. The mobilities in silicon are quite high and therefore suited for the use as *High Energy Physics* (HEP) detectors. The mobility for electrons and holes is $\mu_e = 1350 \text{ cm}^2/\text{Vs}$ and $\mu_h = 450 \text{ cm}^2/\text{Vs}$, resulting in about 10 ns readout time in around 100 μm thick silicon. In material

dominated by one type of impurity, e.g. the donor dopant density N_d is much larger than the intrinsic carrier concentration, the following expression for the resistivity is valid:

$$\rho = \frac{1}{e(\mu N_d)} \quad (1.9)$$

This is a very important parameter, which has to be carefully chosen for sensors. It will be shown later that it is inversely proportional to the detector operation voltage. Generally, high resistivity (5–10 k Ω cm) material is preferred, but low³ resistivity (1–3 k Ω cm) material was chosen for the CMS experiment at the LHC (see Sect. 5.1.1).

So far, the number of free charge carriers and the neutrality of the solid object are considered only in a static way. In the real device there is a dynamic equilibrium. Electron–hole pairs are generated and recombine all the time, only the average concentration remains constant.

Figure 1.2 is more educational than representative for a real device. In an ideal indirect⁴ semiconductor (like silicon) an excited electron (hole) cannot recombine on its own. A phonon is needed to simultaneously conserve energy and momentum. In a real device the recombination rate is completely dominated by second order effects – additional levels in the forbidden gap (Fig. 1.3). The lifetime τ_L is completely defined by the impurities, like interstitial atoms, such as Fe, Ni, Cu, Au, the dopant atoms, crystal dislocation or grain boundaries:

$$\tau_L = \frac{1}{\sigma v_{th} N_t} \quad (1.10)$$

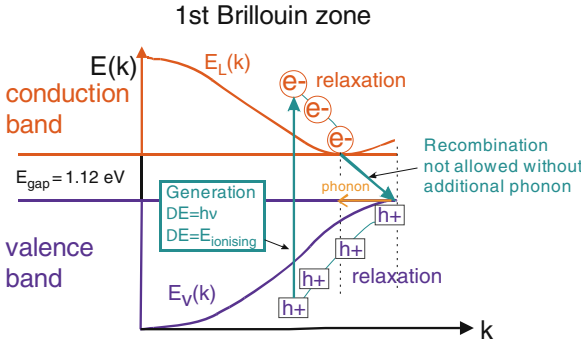


Fig. 1.2 Electron–hole pair generation by a photon in silicon. To obey energy and momentum conservation, recombination is only possible with phonon exchange. Recombination is basically impossible and thus lifetimes τ_L in ideal semiconductors without impurities can range up to milliseconds

³ Not to compare with low resistivity IC silicon material with 10–100 Ω cm.

⁴ The lowest conduction band energy does not lie at the same position in k -space than the highest valence band energy.

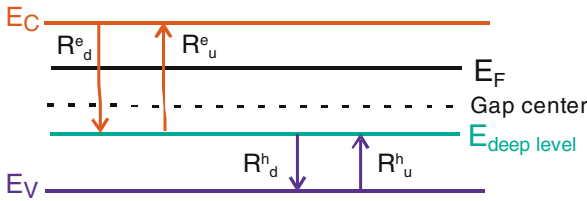


Fig. 1.3 Shockley–Read–Hall in a nutshell: The Shockley–Read–Hall theory describes in detail the second order effects, which in reality are the most relevant mechanisms. Defects take the function of step stones to generate or recombine free charge carriers. Depending on the placement of the levels, reflecting different species of atoms, lifetimes τ_L range from ns to ms.

R_d^e : transit rate of electrons from conduction band to deep level; electron capture

R_u^e : transit rate of electrons from deep level to conduction band; electron emission

R_d^h : transit rate of holes from valence band to deep level; hole capture

R_u^h : transit rate of holes from deep level to valence band; hole emission

with v_{th} as the thermal velocity ($\approx 10^7$ cm/s), the charge carrier cross section σ ($\approx 10^{-15}$ cm²) and impurity/trap concentration N_t .

The important message from the Shockley–Read–Hall theory (schematically displayed in Fig. 1.3) is the function of the impurities, acting not only as traps but also as sources of free charge carriers. The direct band to band ($E_C \leftrightarrow E_V$) generation or recombination is technically negligible. Dislocations or precipitates in the active device regions or point defects in the silicon crystal and especially metal impurities like Cu, Au, Fe, Cr, etc. introduce new levels inside the band gap. This leads to a reduction of minority carrier lifetime and thus influences device characteristics.

Shortly, the influence of τ_L on the intrinsic leakage current of silicon sensors will be introduced.

1.1.2 The pn-Junction

In an intrinsic silicon substrate – the size of a standard silicon sensor used in high-energy physics – there are $\sim 10^9$ free charge carriers but *only* $\sim 2 \times 10^4$ generated electrons induced by an ionizing particle. The resulting signal would be lost in the number of free charge carriers. Therefore, the free charge carriers have to be reduced by several orders of magnitude. This could be achieved by cooling to very low temperatures or by depleting the silicon volume of free charge carriers, using *p*- and *n*-type silicon in a *reverse-biased pn-junction* configuration.

Cryogenic cooling would be highly unpractical for large detector applications, therefore the basic diode properties of a *pn*-junction are exploited. The scope here only describes a *pn*-junction in equilibrium and the actual use of high-doped material in reverse bias at intermediate temperatures.

The principal concept of depleting a semiconductor volume, thus creating a space charge region (SCR), is visualized in Fig. 1.4. As discussed earlier the Fermi energy in thermal equilibrium must be constant. Nature establishes the equilibrium by

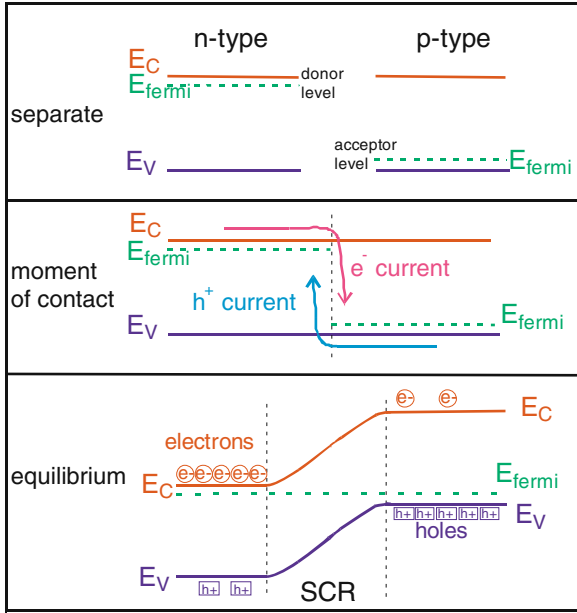


Fig. 1.4 How does p-type behave with its neighbour n-type. By joining p- and n-type together electrons move to the lower Fermi levels and holes to the higher, building up a space charge region (SCR), where in equilibrium, the Fermi energy E_F is constant everywhere. To visualize it, first draw band diagrams for the p and n region separately. Second, join the two parts, the electrons move to the material with the lower Fermi energy, while the opposite is true for the holes. Last, in the state of equilibrium, a space charge is built up and the potentials are shifted accordingly, with the Fermi energy constant everywhere.

the movement of the free majority charge carriers into the opposite regions (electrons move to the p and holes vice versa to the n region) leaving behind ionized charged dopant atoms. The diffusion current j_{Diff} is depicted by Fick's first law $j_{Diff} = -eD\nabla n$, equalizing the carrier density according to its gradient ∇n with the diffusion constant D .

Some basic math is needed to achieve a “feeling” for the device. At the pn -junction diffusion and recombination produces a space charge layer, creating an electrical field $|E|$ and preventing further diffusion. The mathematical expressions are visualized in Fig. 1.5. A dynamic equilibrium is created: diffusion flow and field current of both charge carriers are compensating each other at the pn -junction. The Poisson equation describes the electrostatic potential $\phi(x)$:

$$\frac{\partial^2 \phi}{\partial x^2} = -\frac{1}{\epsilon_{SC}\epsilon_0}\varrho(x) \quad (1.11)$$

Assuming complete ionization the charge density $\varrho(x)$ (Fig. 1.5d) with the impurity densities N_A and N_D (Fig. 1.5b) (acceptor and dopant, respectively) is described by

$$\varrho(x) = -q[n(x) - p(x) + N_A - N_D] \quad (1.12)$$

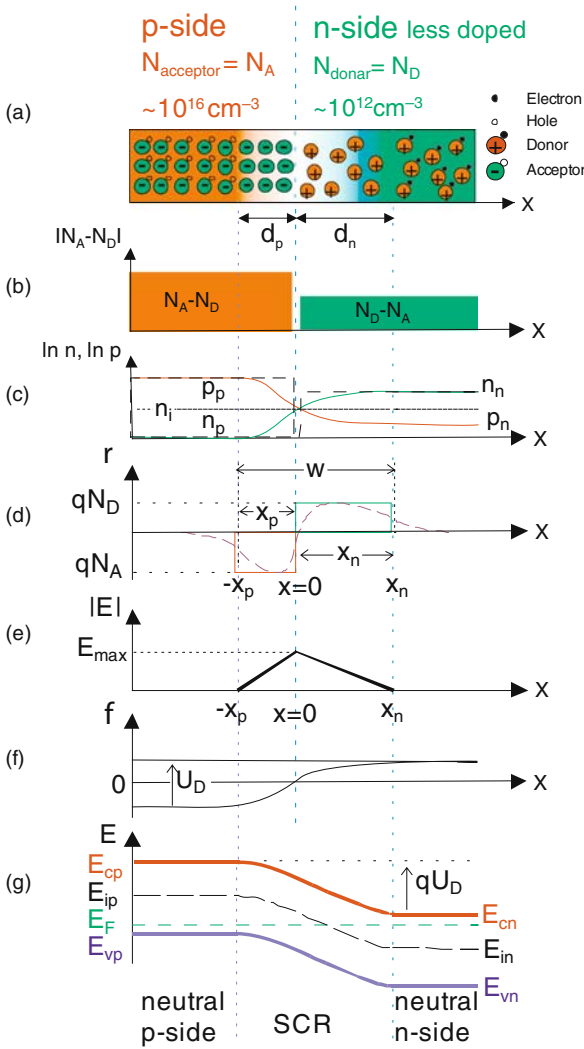


Fig. 1.5 These diagrams display (a) a simple visualization of the atomic and charge configuration, (b) the doping profile, (c) the mobile charge density, (d) the space charge density, (e) the electrical field configuration, (f) the electrical potential, (g) electron energy across the pn-junction. All states are depicting the equilibrium state, without any external voltage

In the very localized contact region of *n*- and *p*-type silicon, the free charges compensate for the charges of ionized and uncompensated impurities.

In Fig. 1.5d the depleted boundary layer is drawn. This leads to the space charge region SCR w :⁵

⁵ Depleted of free charge carriers.

$$w = x_p - x_n \quad (1.13)$$

Integration of the Poisson equation including the depletion approximation⁶ supplies a linear behaviour of the **electrical field strength** $|E|$ (Fig. 1.5e) n -type region $-x_n \leq x \leq 0$ and p -type region $0 \leq x \leq x_p$, respectively, are

$$|E_n(x)| = + \frac{qN_D}{\epsilon_{SCR}\epsilon_0}(x+x_n); \quad |E_p(x)| = + \frac{qN_A}{\epsilon_{SCR}\epsilon_0}(x-x_p) \quad (1.14)$$

Integrating twice leads to the parabolic behaviour of the **potential** $\phi(x)$ (Fig. 1.5f) with the boundary condition $\phi(x=0) = 0$

n -type region for $-x_n \leq x \leq 0$ and p -type region $0 \leq x \leq x_p$, respectively, are

$$\phi_n(x) = -\frac{1}{2}|E_{max}|x_n \cdot \left[\left(\frac{x}{x_n} \right)^2 + 2\frac{x}{x_n} \right]; \quad \phi_p(x) = +\frac{1}{2}|E_{max}|x_p \cdot \left[\left(\frac{x}{x_p} \right)^2 - 2\frac{x}{x_p} \right] \quad (1.15)$$

The total difference of potential in the space charge region gives the **diffusion or built-in voltage** $V_{diffusion}$

$$V_{diffusion} = \phi_p(+x_p) - \phi_n(-x_n) = \frac{1}{2} |E_{max}| w \stackrel{eq. 1.9, 1.14}{=} \frac{1}{2\mu\epsilon} w^2 \quad (1.16)$$

The whole system is completely defined by the energy barriers. Intrinsically the generation and recombination of charges are in equilibrium and the system is externally stable. Creation of large volumes with pure doping concentration difference is technically impossible; $V_{diffusion}$ is on the order of a few millivolts. An additional technique is needed to increase the SCR-depleted volume.

An **external voltage** $\pm V$ will disturb this equilibrium of spontaneous, generation and recombination of electrons. The external voltage increases or decreases – depending on the polarity – the intrinsic potential barrier of the pn -junction. As a result of the external voltage the depletion width decreases or increases (see Figs. 1.6 and 1.7).

Silicon sensors are operated in reverse bias mode and the forward case will not be considered any further. For the detector case, charge created in the SCR region can be collected at the junction, while charge created in the non-depleted zone recombines with free majority carriers and is lost. Operation conditions, namely voltage $V_{external}$, is therefore such that the full volume is depleted. With $V_{external} = V_{bias} \gg V_{diffusion}$ and Eq. (1.16) w results to

$$w = \sqrt{2\epsilon\mu V_{bias}} \quad (1.17)$$

and vice versa

⁶ Assuming an “abrupt” change of $\varrho(x)$ (see Fig. 1.5d – full line).

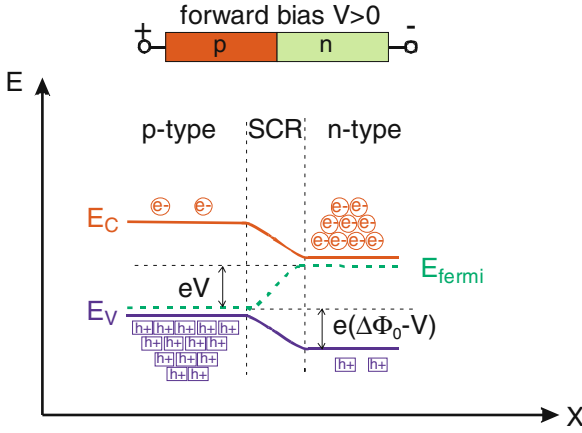


Fig. 1.6 Forward (bias) voltage: In the forward case, the barrier decreases significantly, the majority carriers flow freely through the diode

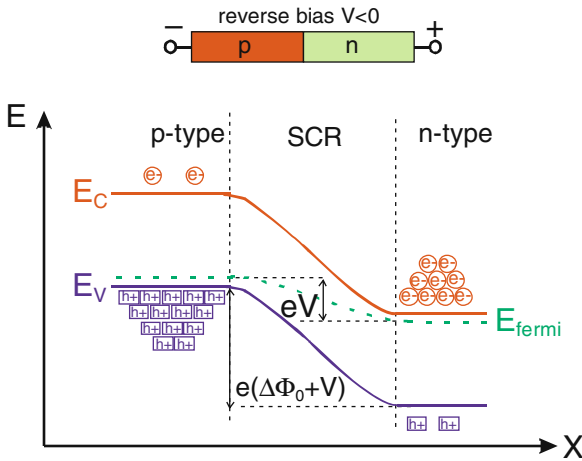


Fig. 1.7 Reverse (bias) voltage: In the reverse bias case, the potential barrier as well as the depletion width increases

$$V_{full\ depletion} = V_{FD} = \frac{D^2}{2\epsilon\mu_Q} \quad (1.18)$$

with $w = D$ as the full sensor thickness. V_{FD} is one of the most important design parameters, describing the minimal operation value – the voltage the sensor has to sustain without going into current breakdown. As an example, the inner CMS sensors are $320\ \mu\text{m}$ thick with a resistivity range of $1.5\text{--}3\ \text{k}\Omega$, the depletion voltage V_{FD} is therefore within

$$V_{FD} = \frac{(0.032)^2 \text{ cm}^2}{2 \cdot (8.85 \cdot 10^{-14} \text{ F cm}^{-1}) \cdot 11.7 \cdot (1350 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}) \cdot (1.5-3) \text{ k}\Omega} \approx 122-244 \text{ V}$$

To run over-depleted the operation voltage V_{bias} is therefore set to 400 V.

Electrical field configurations for under-, full- and over-depletion conditions are shown in Fig. 1.8. The electrical fields for the different external voltage configurations are given by

Under-depletion: $V_{bias} < V_{FD}$

$$E(x) = \frac{2V}{d} \left(1 - \frac{x}{w}\right) \quad \text{with } E_{MAX} = \frac{2V}{w} \quad (1.19)$$

Depletion: $V_{bias} = V_{FD} = \frac{D^2 q_e N_{eff}}{2e}$

$$E(x) = -\frac{q_e N}{\epsilon} (D - x) \quad \text{with } E_{MAX} = \frac{2V}{D} \quad (1.20)$$

Over-depletion: $V_{bias} > V_{FD}$

$$E(x) = \frac{2V_{FD}}{D} \left(1 - \frac{x}{D}\right) + \frac{V - V_{FD}}{D} \quad \text{with } E_{MAX/MIN} = \frac{V \pm V_{FD}}{D} \quad (1.21)$$

With formula (1.21) the maximum electrical fields can be, for example, calculated for a sensor used during the LEP era and one from the CMS time. The bias voltage at DELPHI was set to 60 V with an effective full depletion voltage of 40 V on a 300 μm thick sensor resulting in a minimum electrical field of 666 V/cm and maximum one of 3.3 kV/cm. With $V_{bias} = 400 \text{ V}$ and $V_{FD} = 200 \text{ V}$ applied to a 300 μm thick sensor minimum and maximum electrical field strengths climb to $E_{MIN} = 6.6 \text{ kV/cm}$ and $E_{MAX} = 20 \text{ kV/cm}$.

With $V_{bias} > V_{FD}$, the equilibrium is disturbed and an electrical field is now established, sweeping the thermally generated electron-hole pairs in the SCR G_{SCR} out of the depletion region. As mentioned earlier, the emission process is dominated

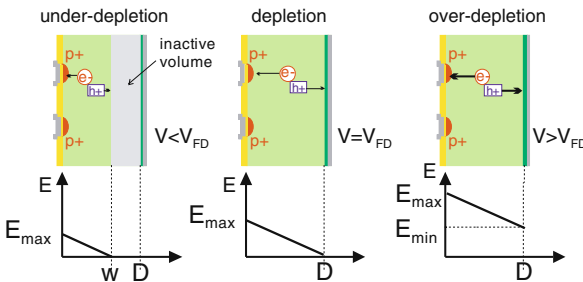


Fig. 1.8 The field in the bulk silicon is linear, depleting a certain volume. The left part shows an under-depleted $V_{bias} < V_{FD}$ sensor, while right scheme shows the standard over-depletion $V_{bias} > V_{FD}$ case, the picture in the middle depicts full depletion $V_{bias} = V_{FD}$: The max field E_{max} is on the segmented side for p-in-n, where the strips are on GND potential and the backplane is on high voltage potential

by the Shockley–Read–Hall transitions. Of course this is now an undesired effect, resulting in a reverse current also called “leakage current” I_L being described by

$$j_R = e \cdot G_{SCR} \cdot w = \frac{1}{2} e \frac{n_i}{\tau_L} w = \frac{1}{2} e \cdot n_i \cdot \sigma \cdot v_{th} N_t \cdot w \quad (1.22)$$

and with the surface A of the junction

$$I_L = \frac{1}{2} e \frac{n_i}{\tau_L} w \cdot A = \frac{1}{2} e \cdot n_i \cdot \sigma \cdot v_{th} N_t \cdot w \cdot A \quad (1.23)$$

In summary, the leakage current is completely dominated by the effective lifetime τ_L (refer to formula (1.10), the generation lifetime of minority carriers), namely the impurity states N_t near mid-gap, e.g. Au and all novel metals are “lifetime killers”, see Fig. 1.1. The temperature dependency enters indirectly via $n_i \propto e^{\frac{E_g}{2kT}}$.

For example, a CMS sensor has a leakage current of ~ 0.5 nA/strip at room temperature, where a strip is $A = 100 \times 0.05$ mm with a depletion width of $300 \mu\text{m}$, the sensor thickness.

$$\tau_L = \frac{1}{2} e \frac{n_i}{I_L} w \cdot A = \frac{0.5(1.6 \cdot 10^{-19} \text{ C})(1.45 \cdot 10^{10} \text{ cm}^{-3})(0.03 \cdot 10 \cdot 0.006 \text{ cm}^3)}{0.5 \cdot 10^{-9} \text{ A}} \sim 4 \text{ ms}$$

The impurity concentration N_t then amounts to

$$N_t = \frac{1}{\sigma v_{th} \tau_L} = \frac{1}{10^7 \cdot 10^{-15} \cdot 4 \cdot 10^{-3} \text{ cm}^3} = 0.25 \cdot 10^{11} / \text{cm}^3$$

The current increases linearly with $w \propto \sqrt{V}$ until the detector is fully depleted. At higher bias voltage an electrical breakdown is observed, where the current starts to increase dramatically. The breakdown can either be explained by “avalanche breakdown”, due to charge multiplication in charge collisions with the lattice or by “Zener breakdown”, based on the quantum mechanical “tunnel effect”. Figure 1.9 shows $I \propto \sqrt{V}$ behaviour, as well as a breakdown. In Chap. 5 a design is introduced, which allows sensor voltages above even the maximum electrical field of silicon.

The full capacitance of a sensor can be calculated by regarding the two planes of the SCR as plates capacitor with silicon as dielectric inside. C decreases linearly with w and therefore $\sim \sqrt{V}$:

$$C_{bulk} = \begin{cases} A \sqrt{\frac{\epsilon_{Si}}{2q\mu V_{bias}}} & V_{bias} \leq V_{FD} \\ A \frac{\epsilon_{Si}}{D_{depletion}} = const. & V_{bias} > V_{FD} \end{cases} \quad (1.24)$$

Figure 1.10 expresses the C and V_{FD} dependency on area, thickness and q . The capacity–voltage characteristic CV or $1/C^2$ vs. voltages behaviour is used as a standard method to determine V_{FD} . The kink determines V_{FD} .

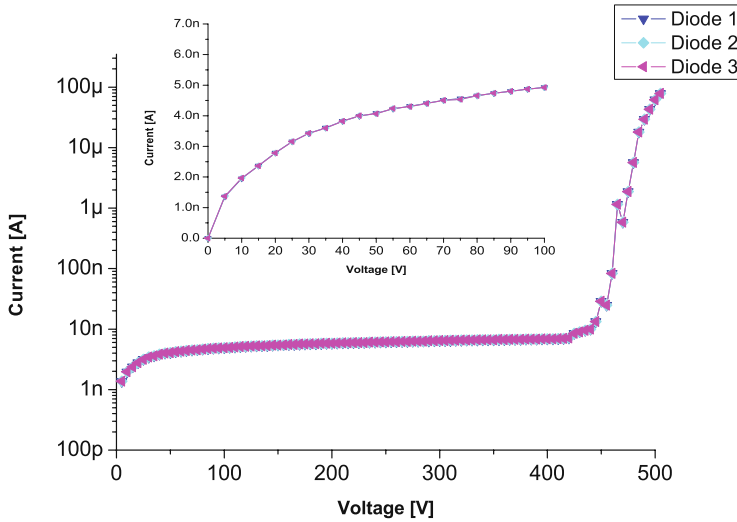


Fig. 1.9 The current–voltage characteristic for a Si diode in the reverse bias direction is depicted. The expanded view shows the $I \propto \sqrt{V}$ dependence, while the global view shows the full scan including breakdown at higher voltages

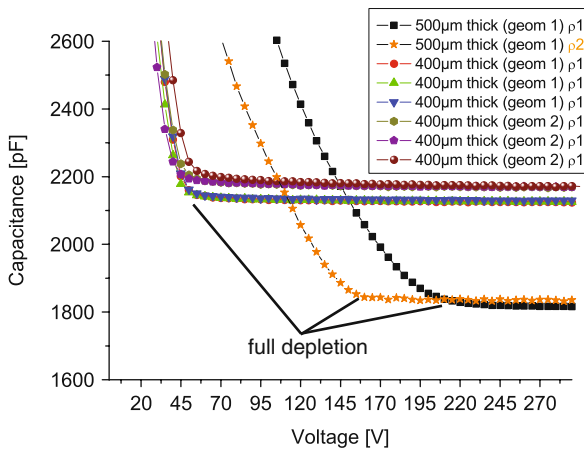


Fig. 1.10 The measurement plots describe the capacitance dependence on area and thickness quite clearly. The x-axis coordinate of the kink shows the depletion voltage, defined by material resistance and thickness. The y-coordinate of the plateau shows the minimal capacitance, defined by area and thickness. The two upper bands depict sensors of two different geometries with slightly different areas and same high resistivity material, both $d = 400\mu\text{m}$ thick. The lower CV curves describe $d = 500\mu\text{m}$ thick sensors. With increased thickness, C becomes smaller and $V_{\text{depletion}} \propto D^2$ becomes larger. The different depletion voltages of the lower curves derive from two different resistivities $\rho_2 > \rho_1$

1.1.3 SiO_2

Silicon oxide SiO_2 is very stable and chemically inert. It is a near-perfect dielectric and one of the best insulators, with an extremely high breakdown field strength. Only the co-existence of Si and SiO_2 defines the real technological value. Pure silicon is simply too chemically reactive, without a thin layer of SiO_2 it will react with anything. The excellent electrical properties of the Si-SiO_2 interface are also very important. This interface has a very low density of energy states in the band gap and therefore neither provides recombination centres nor introduces fixed charges.

SiO_2 is used as

- gate oxide for transistors
- dielectric in capacitors
- passivation and protection
- structure masking during etching, diffusion and ion implantation
- insulation

For tracking sensors it serves mainly as coupling capacitor oxide and as final passivation. Figure 1.11 shows the passivation of all Si areas leaving metal pads free for connectivity.

The growth, application and structuring of SiO_2 are relatively easy and will be described in Sect. 1.8.2, especially how the selective etching possibilities of Si or SiO_2 allow dedicated processing.

Si- SiO_2 Interface

In modern silicon microstrip sensors, the surface consists of a sandwich of high-doped silicon strips, a SiO_2 insulation layer with metal strips on top to be connected

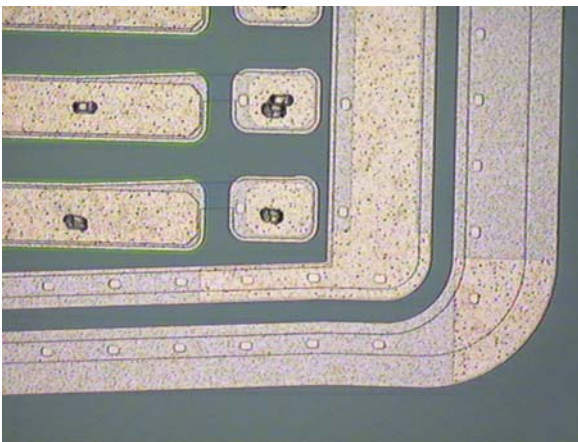


Fig. 1.11 The picture shows a small section of a CMS sensor, where the metal pads are “open” for connectivity, while the rest are all covered with SiO_2 for protection

to the readout electronics, called AC coupling. This *metal–oxide semiconductor* forms the classical MOS structure. The subject is widely discussed for example in [111] or in any electronic or solid state physics literature. The basics are discussed with an emphasis on the importance of a very pure oxide to have a well-defined deep depleted surface for a good strip isolation. The Si–SiO₂ interface condition is defined by the oxide charge or voltage potential applied on the metal part, being simply two aspects of the same physical electron/hole attraction or repelling mechanism. The mechanism acts on the majority carriers of the bulk silicon. The basic cases and their potential structures are diagrammed in Fig. 1.12, they are flat-band condition, accumulation, surface depletion and surface inversion. In Sect. 1.10.2 surface property change with radiation is discussed.

The SiO₂ layer is considered as a thin surface with a constant homogeneous charge density ϱ , the integrated sum of electrons, holes, ionized doping atoms or undesired contaminations.

As for the *pn*-junction, the Poisson equation almost describes the field and band interface situation, only without any net current in the insulator.

The Fermi level E_F is constant, no charge carriers from the semiconductor can neutralize the charges. The surface charges cause an electrical field penetrating into the Si-bulk bending the energy bands.

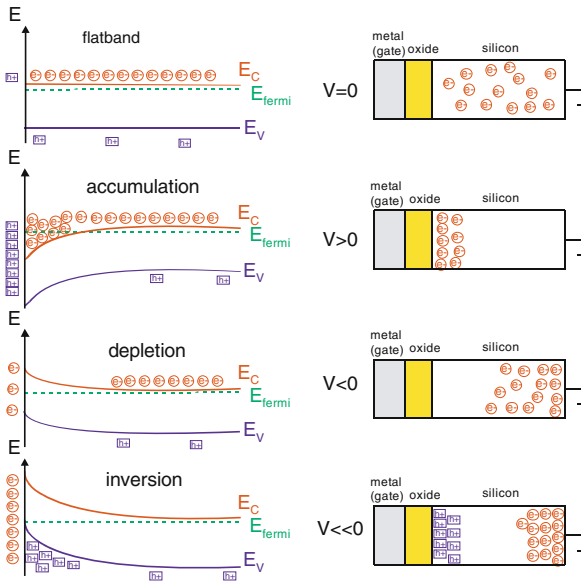


Fig. 1.12 The diagrams show the different optimal cases of a MOS structure: (a) Flat-band, (b) accumulation, (c) surface depletion and (d) inversion. The left part of the diagram schemes the energy bands of the Si–SiO₂ interface taking into account the present charges or potential on the oxide side (no metal), independent of the charge's (potential's) origin. The right part displays a more volume-based picture, with a defined metal gate, where the metal potential defines the interface case. In summary the band structure is defined by energy band shifts originating from voltage or fixed charges on the SiO₂ side

Two majorly different configurations have to be discussed: the surface charge has the same polarity as the bulk majority carriers, the majority charge carriers are driven into the bulk. When a space charge layer builds up, this case is called **surface depletion**, the mandatory case for a HEP sensor. It guarantees the isolation between adjacent strips. Without a possible compensating current, but at a constant E_F the bands are bent. $E_C - E_F$ increases towards the surface. With a very low majority carrier concentration, scaling as $e^{-(E_C - E_F)}$ at the interface, the minority carriers concentration increases due to the mass action law, finally becoming the majority carriers. This configuration is called **surface inversion** and can ruin the strip-to-strip isolation.

In the second configuration, charges from the bulk are attracted to and accumulate at the interface, due to the different polarity in the surface layer compared to the majority carrier in the bulk. The bands are then bent inwards. This case is called **accumulation** and of course also short-circuits neighbouring strips. One prominent example, where an electron accumulation layer forms, is the $n++$ face of a double-sided sensor. There the $n++$ layer attracts electrons at the $n+-n-$ interface. The technical solution for the strip-strip isolation in this case is presented in Sect. 1.6.3. The **flat-band** configuration is the configuration just in between depletion (outward bending) and accumulation (inward bending). In this case, the external charge is just compensating the charge due to intrinsic surface states. The potentials/bands in the silicon bulk are flat.

With an additional metal on top of the SiO_2 layer, the situation changes. The work functions of metal and semiconductor are not the same and the flat-band case is now intrinsically impossible, it can only be achieved via an external voltage, the flat-band voltage $V_{\text{flat-band}}$. In reality, a low $V_{\text{flat-band}}$ is a quality factor of the oxide and refers to a low contamination level. More globally, an external voltage can always shift between the four configurations:

- **accumulation** ($V > V_{\text{flat-band}}$)
- **flat-band condition** ($V = V_{\text{flat-band}}$)
- **surface depletion** ($V < V_{\text{flat-band}}$)
- **inversion** ($V \ll V_{\text{flat-band}}$)

With all the above, it has to be taken into account that in standard operation of strip sensors, no voltage is applied to the metal strips. Implant and metal are at almost the same potential and only oxide contamination, charge-up or contamination in the overlaying passivation can change the needed surface depletion case. In short, in a strip sensor undesired charges in the oxide can easily decrease the inter-strip resistance by several orders of magnitude. CCDs on the other hand make use of exactly the possibility of the band shifts, attracting and repelling charges to shift from CCD cell to cell. In the IC industry, the MOS structure is the most important means to open or close a conductive channel, e.g. for a *Field Effect Transistor* (FET).

Dedicated MOS structures on the sensor wafer allow the measurement of the flat-band voltage and therefore provide a means to qualify oxide quality and have hint at oxide thickness. By varying the voltage over a MOS structure, the accumulation

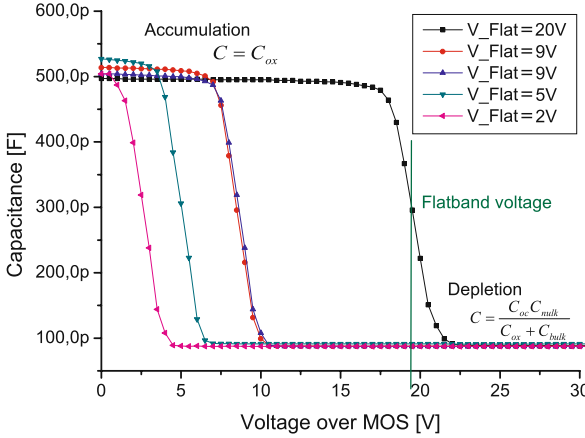


Fig. 1.13 With a capacitance over voltage scan on a MOS structure the point of inflection reveals its flat-band voltage. The flat-band voltage measures oxide thickness and purity. A low value guarantees a low contamination level. High values arise often from significant amounts of oxide traps and/or interface states in the oxide. Levels for HEP sensors range between $V_{\text{flat-band}} = 1$ and 10 V, where the example of 20 V flat-band voltage belongs to a rejected sensor

configuration changes through flat-band case to depletion. In the accumulation configuration the majority carriers are attracted to the surface and the measured capacitance is $C = C_{ox}$, while in inversion case the serial capacitance of oxide plus bulk silicon $C = C_{ox}C_{bulk}/(C_{ox} + C_{bulk})$ is measured. The flat-band voltage marks the inflection of the CV characteristic.

Figure 1.13 displays a CV curve in a MOS measurement with a $V_{\text{flat-band}}$ evaluation of several structures of different quality during the quality assurance campaign of the CMS experiment.

It has to be mentioned that the measurement frequency of the LCR⁷ device plays a role. A high measurement frequency is used to avoid any majority or minority charge carrier movement during the individual C measurement.

1.1.4 Summary of Silicon Properties

To summarize, the properties of intrinsic silicon, the concept of changing electrical properties by adding donor or acceptor atoms were introduced. The connection of p - and n -doped silicon was described, where at equilibrium the Fermi level E_F is constantly forming a potential barrier and a space charge region SCR. The situation so far describes a single diode, which in reverse bias mode is devoid of free charge carriers and any created charge from ionization in the SCR can be collected at the electrodes.

The Si to SiO_2 affinity allows an easy integration of a capacitive coupling of diode to metal contact, thereby allowing the use of a charge amplifying chip.

⁷ Device measuring L inductance, C capacitance and R resistance.

For a tracking detector further segmentation of these “diodes” is needed. The production of raw silicon wafers is described in Sect. 1.8.1 while the processing steps from wafer to silicon sensor are introduced in Sect. 1.8.2.

1.2 Ingredients to Use Silicon as Detector Basis

All tracking detectors make use of the free charges resulting from the ionization of a passing charged particle in a medium, e.g. gas or a semiconductor. The average charge loss of a charged particle in a medium is described by the Bethe–Bloch formula.

$$-\frac{dE}{dx} = 4\pi N_A r_e^2 m_e c^2 z^2 \frac{Z}{A} \frac{1}{\beta^2} \left[\frac{1}{2} \ln \left(\frac{2m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2} \right) - \beta^2 - \frac{\delta(\gamma)}{2} \right] \quad (1.25)$$

In this formula z is the charge of the incident particle, T_{max} the maximum kinetic energy which can be imparted to a free electron in a single collision, I the mean excitation energy, Z the atomic number, A the atomic mass, N_A the Avogadro’s number, m_e the electron mass, c speed of light, r_e classical electron radius, $\beta = v/c$ and $\gamma = \frac{1}{\sqrt{1-\beta^2}}$ and δ density effect correction. The full function of average energy loss of a traversing charged particle is given in Fig. 1.14. The most prominent part is the minimum at approximately $\beta\gamma = 3$, expressing the minimum of deposited energy in the medium. Every detector must be able to keep its noise well below this energy to be able to detect these *Minimum Ionizing Particles* (MIPs).

In addition, there are statistical fluctuations, a subject investigated in depth by Landau. The number of collisions in a finite medium as well as the energy transfer per scattering varies. The first effect can be described by a Poisson distribution, while the latter is described by a “straggling function” first deduced by Landau. In rarer cases, called δ -rays or δ -electrons, the transferred energy is large, these δ -electrons are responsible for the asymmetric long tail towards high charge deposits. All in all the most probable value of energy transfer is about 30% lower than the average value. For silicon, the average energy used for the creation of one electron–hole pair in the indirect semiconductor is 3.6 eV, about three times larger than the band gap of 1.12 eV, deriving from the fact that part of the deposited energy is used for phonon creation. For a MIP the most probable number of electron–hole pairs generated in 1 μm of silicon is 76, while the average is 108. A resulting Landau distribution is shown in Fig. 1.15.

Whereas gas detectors utilize charge amplification in electron avalanche clouds by applying high voltages, solid state devices have to cope with the raw signal of the primary ionization.⁸ About 3.6 eV is needed to create an e–h pair. The high density ($\rho = 2.33 \text{ g/cm}^3$) of silicon causes an average energy loss of about $390 \frac{\text{eV}}{\mu\text{m}}$ for a

⁸ (1) DEPEFTs are silicon sensors with intrinsic amplification, they are introduced in Sect. 1.11.5.

(2) There are also photo-avalanche diodes and silicon photo-multiplier with intrinsic charge amplification, but these are not used as segmented sensors for high energy tracking sensors.

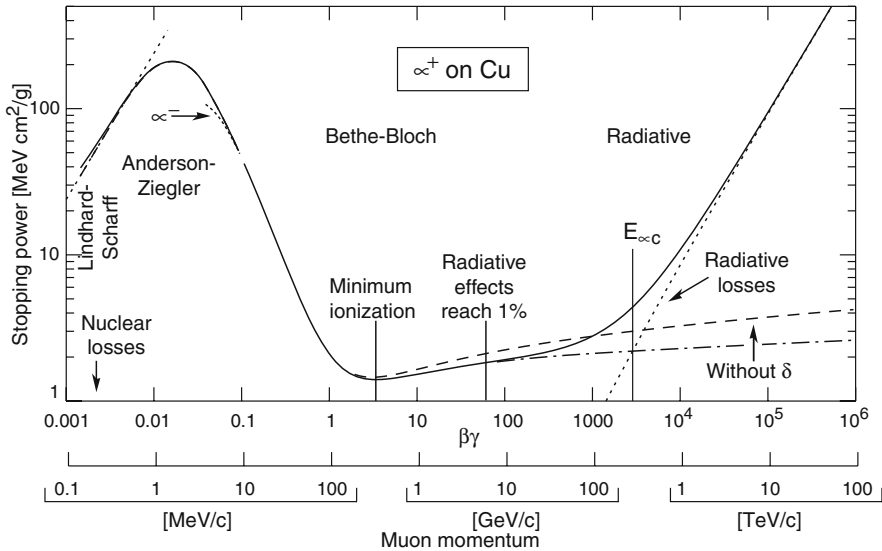


Fig. 1.14 Charged particles lose energy, when traversing material. The figure shows the stopping power $\langle dE/dX \rangle$ of copper for traversing muons [149]. Exactly this effect is the fundamental principle of all ionizing detectors. The sensor design needs to make sure to detect the *Minimum Ionizing Particle* (MIP) with an energy ~ 300 MeV/c with a significant signal/noise (S/N) ratio. The plot includes the corrections to the Bethe–Bloch formula at low and high energies, whose explanations are beyond the scope of this book

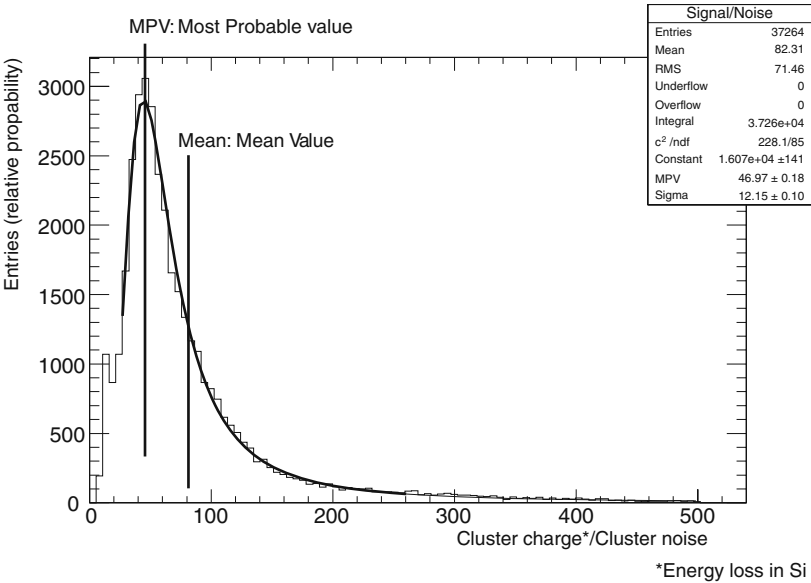


Fig. 1.15 A Landau distribution. The distribution displays ionized charge over noise in 500 μ m silicon from cosmic particles ($\approx$ MIP) arriving at low incident angle in a 3.8 T field. The distribution shows exemplary the difference between *Mean Value* (MV) and *Most Probable Value* (MPV), also the fairly un-symmetric tail of the distribution from δ -rays is clearly visible [153]

MIP, resulting in $108 \frac{e-h}{\mu m}$. In a standard volume of $1 \times 1 \times 0.3 \text{ cm}^3$ at room temperature, there are about 4.5×10^8 free charge carriers vs. 3.2×10^4 electron-hole pairs created by a MIP, this explains the need to work with fully depleted sensors. Due to the Landau fluctuations and the most probable signal of 22,500 electron-hole pairs = $0.7 \times 32,000$, the most probable collected charge is therefore 22500 holes or⁹ electrons collected at either side of the detector equal to 3.6 fC.

1.3 Working Principle of a Silicon Tracking Device

A basic overview of silicon sensors can be found in [133]. The working principle of a silicon microstrip detector is illustrated in Fig. 1.16. An ionizing particle penetrates through a fully depleted silicon n -doped slice. The generated holes drift along the electrical field, created by the bias voltage, to the P+N doped strips¹⁰ while the electrons drift to the $n+$ backplane. Figure 1.8 on page 12 expresses the need to over-deplete to collect holes from the whole volume and to enforce a fast drift to the electrode. The charges collected on the doped strips are then induced, by capacitive coupling, to the aluminium readout strips, which are directly connected¹¹ to the charge preamplifier of the readout chip. In principle, the capacitor does not need to be implemented on the wafer, it can also be instrumented inside the readout chip or in between, this was for example the case for the NA11 experiment, see Sect. 2.2. Sensors with integrated capacitors are called AC coupled and otherwise

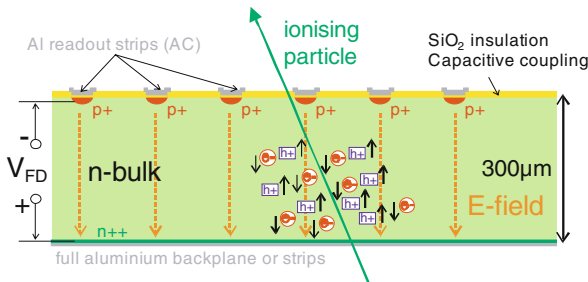


Fig. 1.16 Working principle of an AC-coupled silicon microstrip detector. Electron-hole pairs resulting from the ionization of the crossing charged particle, according to the Bethe-Bloch formula, travel to the electrodes on the sensor planes. The segmentation in the pn-junctions allows to collect the charges on a small number of strips, where they capacitively couple to the Al readout strips. These are then connected to the readout electronics, where the intrinsic signal is shaped and amplified. In the case of segmented p strip implants in an n-bulk silicon material, holes are collected at the p+ strips

⁹ In the most common sensor p-in-n, holes are collected at the segmented side, but for n-in-p, n-in-n or double-sided sensors electrons are also collected.

¹⁰ In an n-in-n, n-in-p or a double-sided detector, electrons drift to the n^+ doped strips.

¹¹ Most often by ultrasonic wire-bonding.

DC coupled. Because the capacitor needs to be large, the full strip length consists of a $p+$ oxide metal sandwich for example in the DELPHI (Chap. 3), CDF (Chap. 4) and CMS experiments (Chap. 5). The final position of the penetration is then calculated by analysing the pulseheight distribution on the affected strips (see Fig. 1.17). A top view photo of a sensor with descriptions of the diverse sensor elements is presented in Fig. 1.18. Figure 1.19 displays a 3D view of a standard single-sided sensor design.

The strip pitch is a very important parameter in the design of the microstrip sensor. In gaseous detectors with a high charge multiplication a signal distribution over several sense wires is welcome to reconstruct the shape of the charge distribution and find the centre. In silicon detectors there is no charge multiplication and small charges would be lost in the noise distribution. Therefore, signal spreading over many strips could result in a loss of resolution. For single-strip events the track position is given by the strip number. The charge cloud on the way to the electrodes also diffuses in the lateral direction. Quantitatively this is mainly affected by bias voltage and temperature. The maximum time available for the lateral drift is the time to travel across the full volume. It can be calculated by $t_{e,h} = d/v_{e,h} = d/\mu_{e,h}E$ with the speed defined by $v_{e,h} = \mu_{e,h}E$. Typical values are thickness $d = 300\mu\text{m}$, mobilities $\mu_e = 1350\text{cm}^2/\text{Vs}$ and $\mu_h = 450\text{cm}^2/\text{Vs}$, mean electrical field strengths $|\langle E \rangle| = 2.5\text{ kV/cm}$ (DELPHI) or $|\langle E \rangle| = 15\text{ kV/cm}$ (CMS). For these example parameters resulting lateral drift times are subsequently $t_e = 9\text{ ns}$ and $t_h = 27\text{ ns}$ (DELPHI) or $t_e = 1.5\text{ ns}$ and $t_h = 4.5\text{ ns}$ (CMS). With diffusion $\sigma = \sqrt{2Dt}$ and the diffusion constant $D = \mu k_B T/q$, temperature dependence comes into play and the charge cloud diffusion for electrons and holes is the same, because μ cancels with $t \propto 1/\mu$. This results in a diffusion of approximately $6\mu\text{m}$ in the LEP era running detectors at room temperature and below $1\mu\text{m}$ in the CMS experiment operating at $T = -20^\circ\text{C}$ and lower temperature. For tracks generating enough charge on two strips to exceed the threshold value, the position can be determined more precisely by either calculating the “center of gravity”¹² or by using an algorithm that takes into account the actual shape of the charge distribution¹³ and the acceptance of the sensor. The best localization is achieved for tracks in the middle of two strips, since the charge is shared equally and the influence of noise is small. The signal for tracks near one strip have poor localization properties, because the remaining small signal on the neighbouring strips is often in the range of or below the noise level. The “center of gravity” method, illustrated for two strips involved, makes use of the parameter η where

$$\eta = \frac{PH_L}{PH_L + PH_R} \quad (1.26)$$

PH_L and PH_R are the pulseheights measured on the left and right strip, respectively. The position is then calculated as

¹² Assuming a uniform charge distribution, a track crossing between two strips at $\frac{3}{4} \times \text{pitch}$ will store $\frac{1}{4} \times \text{charge}$ on the left strip and $\frac{3}{4} \times \text{charge}$ on the right strip.

¹³ Approximately a Gaussian distribution, due to the diffusion profile.

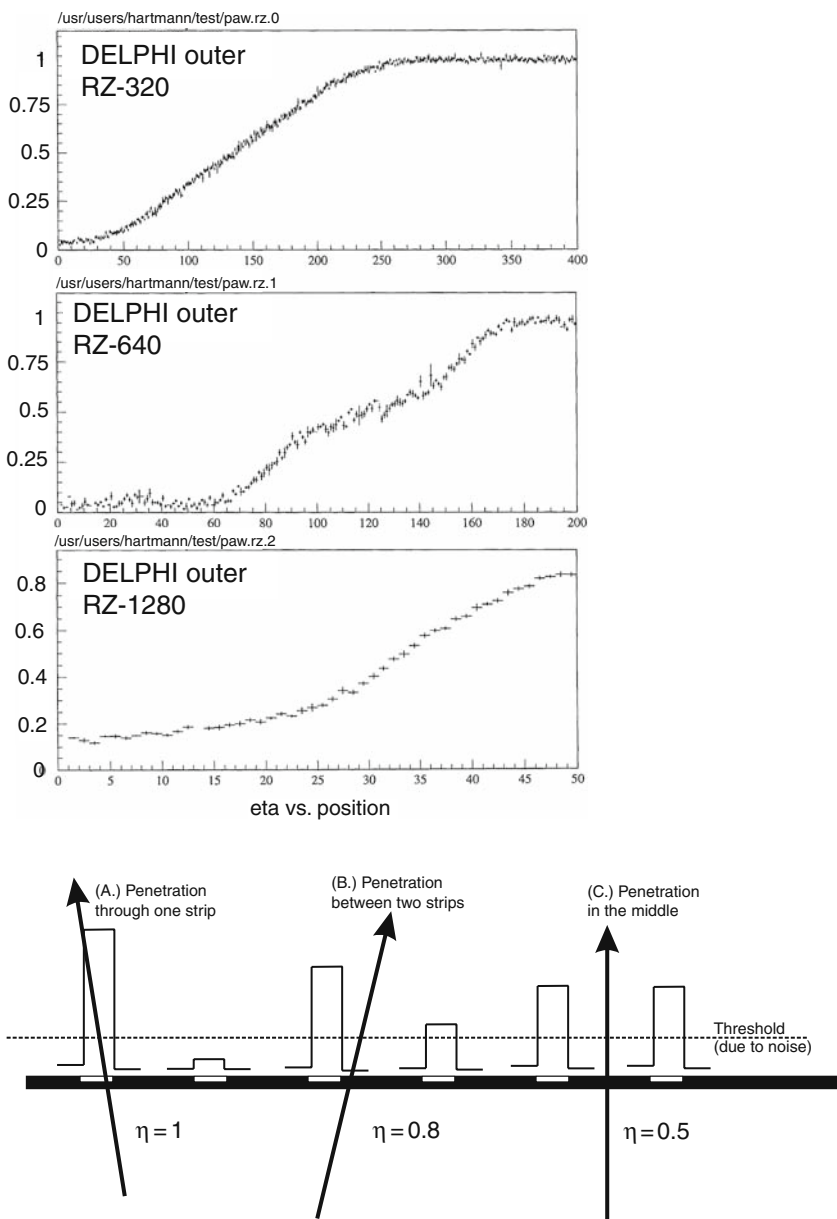


Fig. 1.17 Cluster shape depending on particle location. (A) shows a single-strip cluster, the complete charge is collected on one strip; (B) displays a two-strip cluster the second strip signal lies just above the threshold. (C) A distinctive charge distribution provides best localization precision. In the upper part, the η function is plotted against the position of a red laser hit for the three different sensor types of the DELPHI outer detector with 50, 100, 200 μm pitch for sensors RZ1280, RZ-640 and RZ-320, respectively. The x-axis counts laser steps of $0.5 \mu\text{m}$ [78]

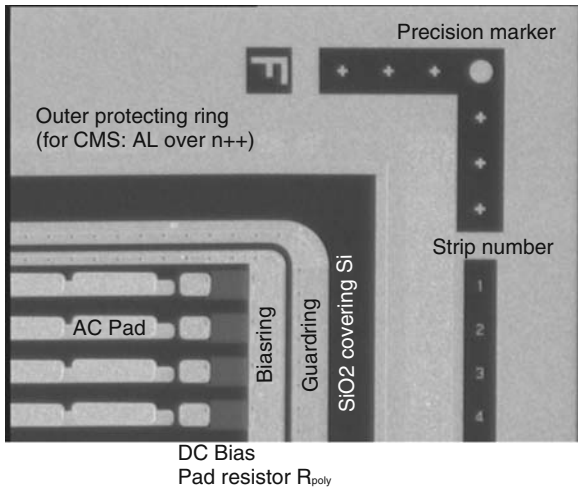


Fig. 1.18 The top view of a sensor, the ring structures, like $n++$ active edge protecting ring, guard ring and bias ring are easy to spot. Both guard and bias rings are Al structures located on top of the $p+$ implants, they are directly contacted. Precision markers are needed to enable a precision assembly, while the strip numbers facilitate problem reports during quality assurance. The bias resistors connect the $p+$ strip located below the aluminium strips to the bias ring. A number of AC pads are processed at the end of the strips to enable several connections to the readout electronics. The DC pad, a direct contact to the $p+$ strip, enables probing

$$x = x_{strip1} + \frac{PH_2}{PH_1 + PH_2} (x_{strip2} - x_{strip1}) = \frac{PH_1 \cdot x_{strip1} + PH_2 \cdot x_{strip2}}{PH_1 + PH_2} \quad (1.27)$$

with a resolution of

$$\sigma_x \propto \frac{\text{pitch}}{\text{signal/noise}} \quad (1.28)$$

As a result, sensors with a pitch of $p = 25\mu\text{m}$ and a signal/noise (S/N) of 50 have a position resolution of $2\text{--}4\mu\text{m}$. Additional intermediate implant strips in between readout strips improve the resolution further by capacitively coupling to the readout strips. This technique helps to minimize number of electronic channels while achieving an adequate position resolution.

For digital readout, the position resolution is given by $\sigma_x \approx p/\sqrt{12}$.¹⁴

Design parameter values for the different structures like bias resistors and coupling capacitances for the different needs of different vertex detectors are presented in the following sections. Also structures like guard rings, bias rings, $n++$ rings, etc. will be discussed.

¹⁴ $\sigma_x \approx p/\sqrt{12}$ arising from geometrical reflections: $\langle \Delta x^2 \rangle = \frac{1}{p} \int_{-p/2}^{p/2} x^2 dx = \frac{p^2}{12}$.

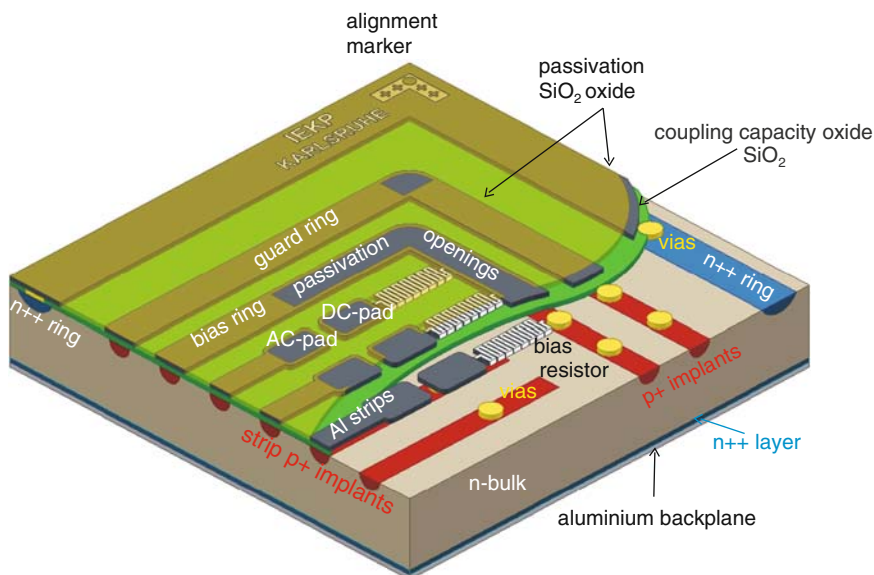


Fig. 1.19 A 3D schematic is sketched. It shows the baseline of the CMS sensor at the LHC in 2008, but could represent basically any single-sided AC-coupled, R_{poly} biased sensor. In operation, the bias ring is connected to GND potential, which is then distributed to the p+ implant strips, while the Al backplane is set to positive high voltage depleting the full n-bulk volume by forming a pn-junction p+ strip to n-bulk. The coupling capacitor is defined between aluminium strip and p+ implant, the inter-strip capacity between neighbouring strips (both p+ and Al part). The guard ring shapes the field at the borders. The n++ ring defines the volume and prevents high field in the real cut edge regions

All individual isolated strips need to be at the same potential. This is realized in one of three different ways, illustrated in Fig. 1.20, although nowadays the polysilicon method is most utilized.¹⁵

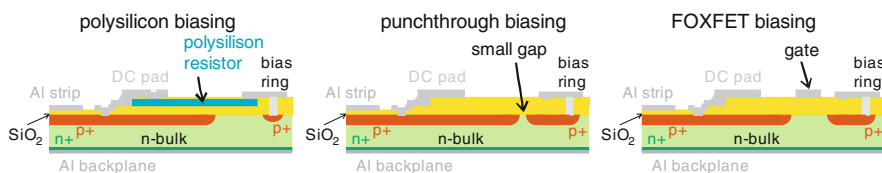


Fig. 1.20 There are three ways to bias an AC-coupled sensor plus a fourth one for a DC-coupled device. The punchthrough and FOXFET biasing are the easiest ones but not as radiation hard as the polysilicon resistor, which is more or less the current standard. A photo of a polysilicon resistor can be seen in Fig. 1.28. In addition, a DC-coupled device can be biased via the connections to the electronics, representing the ground potential

¹⁵ Punchthrough and FOXFET biasing is less radiation hard, it can be imagined for the future International Linear Collider (ILC).

1.4 Single Sided–Double Sided, Double Metal

So far, only single-sided sensors have been introduced. Segmentation of the bulk silicon material can be done on both sides with many benefits but also many additional problems. The obvious benefit is a 2D readout with different strip orientation on each side¹⁶ of a single sensor. Strip implants are then composed of $p+$ and $n+$ on the two sides, named junction and ohmic side, respectively. The ohmic side, with $n++$ strips in an n -bulk, needs special attention to arrange strip isolation due to the presence of an electron accumulation layer with additional $p+$ doping in between $n+$ strips or electron-repelling field plates (Sect. 1.1.3 (accumulation layer at the $Si-SiO_2$ interface) and Sect. 1.6.3 (isolation strategies for n -in- n readout)). An exemplary case is presented in Fig. 3.11 on page 116, where the DELPHI double-sided sensors are discussed. Double-sided processing is briefly discussed in Sect. 1.8.2. Several additional processing steps are needed and in several cases, the sensor faces are not completely independent, as a critical example on page 92 in Sect. 1.1.3 for the CDF experiment proves. Production yield is a key issue with double-sided sensors. In many cases, the second side needs an additional routing layer to lead the signals from the implants to the readout electronics. The routing is normally realized via an additional isolation layer in combination with another layer of aluminium routing strips connected individually by vias to the implants (see Fig. 3.10 and Fig. 3.11).

1.5 Noise Contributions

Even for a fully depleted sensor bulk volume, sources of statistical electron and hole fluctuations exist. These fluctuations, called noise, are counter-productive and compete with the signal from the traversing ionizing particles. The sources are manifold and of different severity for the diverse operation conditions and readout strategies. A strong dependence on the peaking time t_p and operating temperature T exists. With signal to noise (S/N) being the figure of merit of a sensor, noise must be minimized while signal can only be increased by increasing sensor thickness. The noise contributing elements are load capacity C_d , leakage current I_L , parallel and series resistances R_P and R_S . A simplified noise scheme is shown in Fig. 1.21. The load capacitance C_d is mostly comprised of the inter-strip and strip to backplane capacitance.

Noise is generally expressed as *Equivalent Noise Charge* (ENC) or Q_n , representing number of electrons contributing to the noise. The different contributions sum up quadratically:

$$ENC = \sqrt{ENC_C^2 + ENC_{I_L}^2 + ENC_{R_P}^2 + ENC_{R_S}^2} \quad (1.29)$$

¹⁶ Common strip orientations are 90° or a small stereo angle like $0.1-2^\circ$

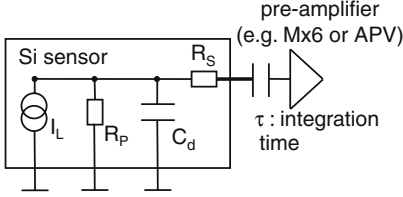


Fig. 1.21 A simplified equivalent network of a sensor together with its preamplifier. The main noise sources leakage current I_L , parallel and series resistance R_P , R_S and load capacitance C_d are shown. Such a diagram is valid per individual strip or pixel

with the *shot noise* term from leakage current

$$ENC_{I_L} = \frac{e}{2} \sqrt{\frac{I_L \cdot t_p}{q_e}} \approx 107 \sqrt{I_L / nA \cdot t_p / \mu s} \quad (1.30)$$

the *parallel thermal noise* term from bias resistance

$$ENC_{R_P} = \frac{e}{q_e} \sqrt{\frac{k_B T \cdot t_p}{2 R_P}} \approx 44.5 \sqrt{\frac{T/K \cdot t_p / \mu s}{R_P / M\Omega}} \quad (1.31)$$

the *serial thermal noise* term from the metal strip resistance

$$ENC_{R_S} = C_d \cdot \frac{e}{q_e} \sqrt{\frac{k_B T R_S}{6 t_p}} \approx 0.025 \cdot C_d / pF \sqrt{\frac{T/K \cdot R_S / \Omega}{t_p / \mu s}} \quad (1.32)$$

and the most significant contribution, the load capacitance

$$ENC_C = a + b \cdot C_d \quad (1.33)$$

where e is the Euler number, k_B the Boltzmann constant, q_e the electron charge, t_p the peaking time and T the operating temperature. The constants a and b , in the ENC_C term, are preamplifier-specific parameters. The slope b is mostly defined by the intrinsic chip voltage noise $u_{n,amp}$ and the peaking time t_p together with a form factor arising from the pulse shape.

$$b \sim \frac{u_{n,amp}}{t_p} \quad (1.34)$$

Vice versa the above-mentioned noise behaviours have direct implications on the design parameters of the sensors. To minimize noise the following sensor design criteria have to be fulfilled:

- small load capacitance $C_d = C_{strip}$ ($\sim$ strip length)
- low leakage current I_L
- high parallel resistance R_{bias}
- small series resistance R_{strip}

These design choices and parameters will be discussed in more detail in the next sections and chapters, e.g. strip length, choice of bias method, sensor quality, etc. Furthermore, the frequency dependence, hence readout method choice, significantly influences the design choices. For example, capacitance tuning is much more relevant for short peaking times ($\sim \sqrt{\frac{1}{t_p}}$), while for larger peaking times noise due to leakage current and bias resistance is more enhanced ($\sim t_p$). Also the temperature is important for both leakage current (*shot noise*), noise (current doubles for $\Delta T \approx 7^\circ\text{C}$) and ENC_{R_P} and ENC_{R_S} (*thermal noise* $\sim k_B T$). Obviously, detectors at the future *International Linear Collider* (ILC), with a longer shaping time will be sensitive to low resistor values and shot noise from leakage current, whereas detectors at the LHC with a very short bunch crossing use a short shaping time, where noise is maximally affected by the ENC_C term. To reduce the peaking time dependency one can use an analog pulse shape processing step after the preamplifier stage and therefore increase the integration time, but the pulse shape processing (deconvolution mode) itself will slightly change the different noise terms [40, 41, 95]. An example on how the different noise terms contribute for different modules and different peaking times is given in Table 1.2 including the modification factors for the deconvolution mode. Some examples of the ENC_C term for different chip versions of DELPHI, CDF and CMS, adapted for different load capacities and different timings, are given in Table 1.3. The three different values for the different stages of the DELPHI experiment represent different chip generations. The large dependence

Table 1.2 The table shows the different noise contributions for a DELPHI and a CMS module. In the quadratic sum, the ENC_C term is the most significant. The higher noise of the CMS module is dominated by the faster peaking time of 50 ns, which mostly determines the slope b in the ENC_C term and the ENC_{R_S} term. To compensate the high noise for long CMS modules, the sensor thickness had to be increased to achieve a higher signal. The shot noise term ENC_{I_L} is suppressed ($I_L = 1 \text{ nA}$). The second ENC_{I_L} value of $756e^-$ for CMS reflects the current increase due to irradiation

Detector	t_p dep	DELPHI microvertex	CMS tracker	
chip		MX6	APV peak	APV deconv
t_p		1.8 μs	50 ns	12 ns, effective
T		20°C		-10°C
C_d		2 $\times$ 6 cm $\rightarrow C_d = 9 \text{ pF}$	2 $\times$ 10 cm strips $\rightarrow C_d = 18 \text{ pF}$	
		a = 340; b = 20	a = 270; b = 38	a = 400; b = 60
$\rightarrow ENC_C$	$\sim 1/t_p$	520 e^-	711 e^-	1480 e^-
I_L		0.3 nA	1 nA to 1 μA	
$\rightarrow ENC_{I_L}$	$\sim \sqrt{t_p}$	78 e^-	24 e^- to 756 e^-	$\times 0.45$
$R_P = R_{bias}$		36 M Ω	1.5 M Ω	
$\rightarrow ENC_{R_P}$	$\sim \sqrt{t_p}$	169 e^-	131 e^-	$\times 0.45$
$R_S = R_{strip}$		25 Ω	50 Ω	
$\rightarrow ENC_{R_S}$	$\sim \sqrt{1/t_p}$	13 e^-	230 e^-	$\times 1.45$
sum ENC		552 e^-	760 e^- to 1073 e^-	1518 e^- to 1556 e^-

Table 1.3 ENC values for the different chip generations.

$$ENC = a + b \cdot C_d$$

MARK II; Microplex $ENC = 280e^- + 97e^-/\text{pF} \cdot C_d$
DELPHI; MX3 $ENC = 670e^- + 55e^-/\text{pF} \cdot C_d$
DELPHI; MX6 $ENC = 340e^- + 20e^-/\text{pF} \cdot C_d$
DELPHI; TRIPLEX $ENC = 283e^- + \mathbf{17e^-}/\text{pF} \cdot C_d$
CDFII; SVX3D $ENC = 500e^- + \mathbf{60e^-}/\text{pF} \cdot C_d$
CMS; APV (Peak) $ENC = 270e^- + \mathbf{38e^-}/\text{pF} \cdot C_d$
CMS; APV (deconv) $ENC = 400e^- + \mathbf{60e^-}/\text{pF} \cdot C_d$

The bold numbers emphasize some important steps, e.g. load capacity adaptations (TRIPLEX) and reductions even for faster shaping times (CDF and CMS).

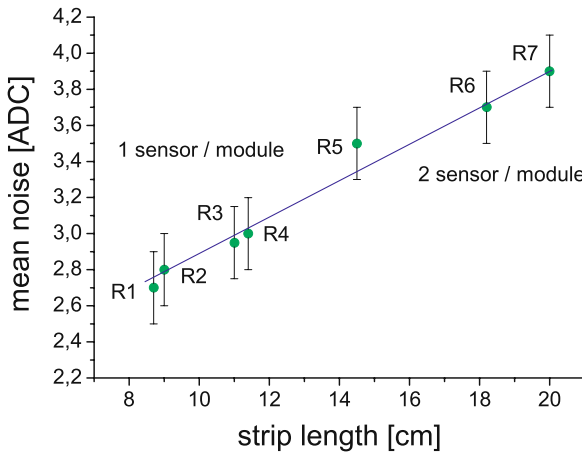


Fig. 1.22 Noise increases with strip length for the different CMS forward detector sensors and module geometries. R1–R7 labels the different rings of the forward with different module lengths

on capacitance for the CMS experiment presents the strong frequency dependence (sampling times: $1.8\ \mu\text{s}$ for DELPHI, $132\ \text{ns}$ for CDF and $50\ \text{ns}$ for CMS). The C_d -dependent value $b = 60e^-/\text{pF}$ for CMS seems to be high, but it is completely driven by the sampling time; compared to the MX3 value one should appreciate the development progress made between the year 1990 and 2000. Obviously the strip length is proportional to the load capacitance C_d , being composed of the strip capacity to its neighbour and to the sensor backside. An example of linear noise dependence vs. C_d (strip length) is illustrated in Fig. 1.22.

1.6 Sensor Parameters

All parameters have to be tailored, specified in detail, validated and monitored according to their specific need, which will be discussed in the following sections. Certain interdependencies must be balanced to achieve best results. In the following,

geometric structures are discussed, including their effects on the functionality like bias and guard ring, implant and Al together with $p+$ strip widths and thickness. Furthermore, the fundamental electrical parameters are introduced to achieve the best operation conditions for the different needs, which are often substantially different for detectors of the last decades and their environment.

1.6.1 Global Parameters

The global sensor parameters, full depletion voltage V_{FD} and total leakage current, are discussed here.

Depletion Voltage ($V_{\text{depletion}} = V_{FD}$)

To ensure full charge collection in the detector, the silicon has to be depleted of free and mobile carriers by applying $V_{\text{bias}} \geq V_{FD}$ in reverse direction. The drift velocities and therefore the drift times and widths of the charge distribution are also affected by the bias voltage. Wider distributions lead to events where the charge is shared between two strips. For these events the center of gravity calculation is possible, having an immediate positive consequence on the position resolution. Micro-discharge is another critical issue, which can be avoided by limiting V_{FD} safely below the micro-discharge voltage.

The depletion layer acts like a parallel plate capacitor, therefore the bulk capacitance per unit area is determined by the depth of the depletion layer w :

$$C_{\text{bulk}} = \frac{\epsilon_{Si}}{w} = \sqrt{\frac{\epsilon}{2\mu\rho V_{\text{bias}}}} \quad (1.35)$$

where ϵ_{Si} is the permeability of the bulk silicon, μ the mobility and ρ the resistivity. Depleting the full sensor $w = D$, formula 1.35 resolves to V_{FD}

$$V_{FD} = \frac{qD^2|N_{\text{eff}}|}{2\epsilon_{Si}} = \frac{D^2}{2\epsilon_{Si}\rho\mu} \quad (1.36)$$

where N_{eff} is the effective charge carrier density, which is the number of donors minus the number of acceptors, and q is the absolute value of the electron charge. After depleting the whole bulk, $w = D$, C_{bulk} will remain constant. This gives a characteristic behaviour C_{bulk} over voltage.

$$C_{\text{bulk}} = \begin{cases} \sqrt{\frac{q\epsilon_{Si}|N_{\text{eff}}|}{2V_{\text{bias}}}} & V_{\text{bias}} \leq V_{FD} \\ \frac{\epsilon_{Si}}{D} & V_{\text{bias}} > V_{FD} \end{cases} \quad (1.37)$$

The value of V_{FD} is directly observable in a CV plot, where C_{bulk} becomes constant and the curve flattens. The absolute V_{FD} mainly depends on the resistivity ρ

and therefore N_{eff} (see also Fig. 1.10 on page 14). The applied voltage also influences the collection time of the ionized electron–hole pairs, which furthermore defines the time of lateral diffusion. The diffusion determines the cluster size of the signal, see discussion on page 22. A deviation of depletion voltage behaviour for segmented devices is briefly presented in Sect. 1.6.3.

Another criterion for a large silicon vertex detector is the ability to apply one single V_{bias} , therefore $V_{FD} \propto D^2 \cdot N_{eff}$ should not vary over the individual sensors. A good uniformity of wafer resistivity is very beneficial. Unfortunately, the direct dependence of V_{FD} on the raw silicon resistivity results in a range of up to 200 V in the CMS experiment, especially for low-resistivity silicon sensors. In the ideal case, V_{FD} should be homogeneous, because several sensors are ganged to one module (e.g. see DELPHI Fig. 3.6 or CDF Fig. 4.14) and only one voltage can be applied, or even worse many modules are connected to one high voltage power supply channel. In addition, the Lorentz angle [50] is dependent on the operation voltage, where track reconstruction requests one single value.

Total Leakage Current ($I_{leakage}$)

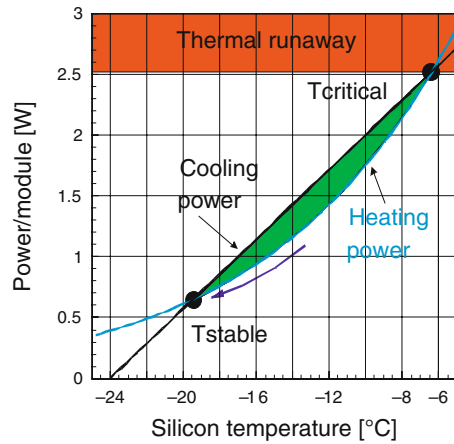
A low total leakage current is one of the major criteria for the quality and functionality of a microstrip detector. Leakage current is a source of noise in a final readout system, which should be kept as low as possible. Leakage current shows up in all detectors coming from generated electron–hole pairs in the silicon in the presence of an electrical field. The leakage current is proportional to the depletion layer thickness d of the sensor which is proportional to $\sqrt{V_{FD}}$. It should be constant after reaching V_{FD} . Deviations from this rule are direct indications of sensor flaws, e.g. variations in processing. Bulk sensor currents are direct indications for bulk impurity concentrations, defining the charge carrier lifetime, thus the current. The leakage current should not exceed a certain limit, excess leakage current results in noise. High current, especially a localized one, is also a defect signature. When measuring the global leakage current, bulk current must be distinguished from surface currents deriving from bad oxides, scratches and/or process errors. Bulk leakage currents are strongly temperature dependent (Sect. 1.1.2), while surface currents are much less temperature dependent. Finding the sources of a high total leakage current could help to improve process methods (see Sect. 1.13).

The strong dependence between leakage currents and temperature leads to an additional critical effect – thermal runaway. Especially after irradiation, sensors have to be cooled to avoid a thermal runaway due to increase of leakage current and voltage – power. Heating power in the silicon can be expressed by

$$P_{silicon} = V_{bias} \times I_{leakage} \sim V_{bias} \times T_{silicon}^2 \times e^{-\frac{0.62\text{eV}}{T_{silicon} \cdot k_B}} \quad (1.38)$$

The system is self-feeding; higher temperature introduces higher current, which vice versa increases power and temperature. Assuming a linear cooling power, a critical temperature limits the stable running. The system overheats, “runs away” above

Fig. 1.23 A thermal runaway. For $T > T_{\text{critical}}$, the system will “thermally run away”, while for temperatures below the critical one $T < T_{\text{critical}}$, the system stabilizes at T_{stable}



T_{critical} , while it stabilizes for $T < T_{\text{critical}}$ at T_{stable} (see also Fig. 1.23). For non-irradiated silicon T_{critical} is well above room temperature.

1.6.2 Bias-, Guard- and Outside Protection Rings

The ring structures surrounding the active area including the sensor outer edge are discussed in this subsection as well as passivation.

Passivation

Passivation is the final step to protect the sensor from the environment. It often consists of a crude form of SiO_2 , sputtered on the sensor or a film of polyimide.¹⁷ Only the bonding and testing areas (Al) are later opened, refer also Fig. 1.11. In contrast to the passivation needs in industry, the material for sensor protection has to be without contaminants. Already small charges can change the well-designed field configuration on the implants and Si-SiO_2 interface, e.g. negative charge concentration can evoke a surface inversion layer, opening a hole conduit from strip to strip decreasing inter-strip resistance. An example of this undesired effect is presented in Sect. 5.2.1.

Bias Ring

The bias ring and backplane are the main contacts to apply the bias voltage. The bias ring runs around the whole active area of the sensor to ensure a homogeneous

¹⁷ Polyimide (sometimes abbreviated PI) is a polymer of imide monomers, it is resilient against ionizing radiation.

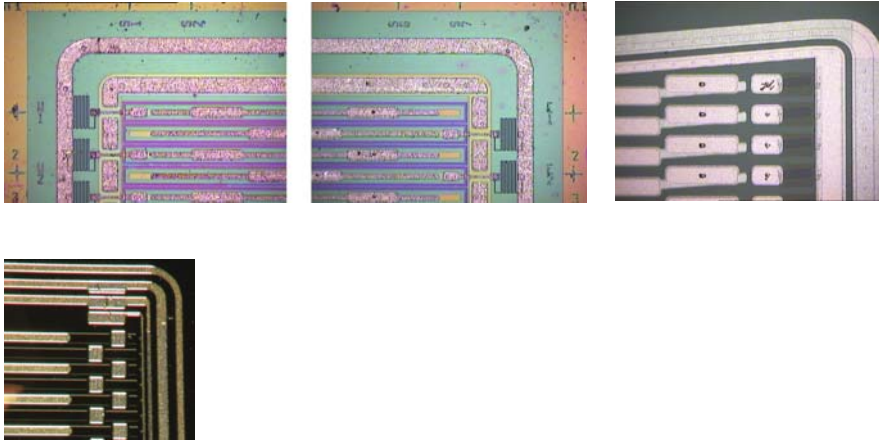


Fig. 1.24 The bias ring connects the strips to a defined potential, e.g. GND on a single-sided p-in-n sensor. The bias ring in the first two photos surrounds the guard ring and connects via polysilicon resistors to the individual strips – DELPHI n -side. On the upper right, a CMS sensor corner can be seen, with the bias ring inside the field shaping guard ring also providing bias potential via polysilicon resistors. On the lower left, a DELPHI ministrip sensor corner is displayed, with (from right to left) two outer guard rings, a bias ring and a gate to control the FET channel /conductivity between bias ring and strips. Note the bond pads for one guard ring, the bias ring and the FOXFET gate

potential for all strips. It either connects to all bias resistors, therefore supplying all implants with voltage, or via the punchthrough effect or FOXFET described earlier. The bias ring is not ultimately necessary for DC-coupled sensors, where the potential can be applied via the readout chip connection. A DELPHI and CMS example with polysilicon biasing plus a FOXFET bias example from DELPHI is displayed in Fig. 1.24. The different biasing schemes are explained in Fig. 1.20.

Guard Ring(s)

The guard ring shapes the field inside the sensitive area to minimize edge effects and guarantees a defined homogeneous potential for all strips, including the edge ones.

Two basic connection schemes can be applied. First, a direct connection of the guard ring to a certain potential, often GND, provides a drain for the leakage currents from the edges of the detector, e.g. applied for the DELPHI sensors. The second configuration uses one or more “floating” guard rings to discretely adapt the potential, especially for high voltages, where the voltage drops from outside in. The ultimate example of a single guard ring serving as multi-guard structure is described in Sect. 5.1.2. For the purpose of field shaping, an implant ring with the same type as the strip implant is located underneath the guard ring. The Al planes and $p+$ implants are directly connected by vias.

Sensor Edges

Cracks caused during the cutting process at the edges introduce energy levels in the forbidden gap. The suppressing of resulting leakage currents can be accomplished by avoiding high field inside the crack region. This can be achieved by the introduction of a new edge $n+$ implantation on the p -side – the $n++$ edge field shaper [131]. This design was first introduced for CDF RUN II and is consequently used in the CMS sensor design.

1.6.3 Design of Strip Parameters

This section illustrates the basic design choices for aluminium readout and implant strips as well as the resulting electrical parameters, like coupling and inter-strip capacitances. Also inter-strip and bias resistances are discussed here. The common strip faults are introduced. The AC-coupling case is described. Figure 1.25 shows an electron microscope picture of a cut through an AC-coupled strip.

Layout of Implants and Aluminium Strips

To define the Al strip implant configuration several things have to be taken into account. In an AC-coupled sensor, the coupling capacity must be larger than the inter-strip capacitance and all parasitic capacitances. In first order the aluminium strip and the implant strip define parallel plate capacitors between themselves, between the Al

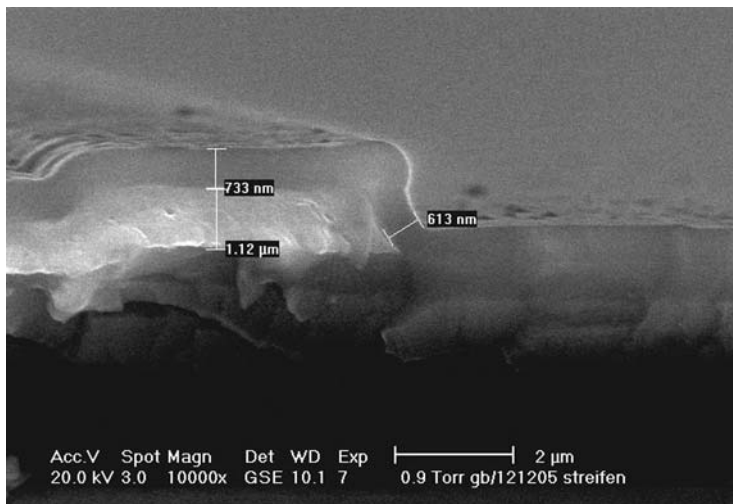


Fig. 1.25 Cut perpendicular through a single strip. The picture shows the upper part, especially the metal part and the passivation oxide protecting it from the environment

strip implant complex and the backplane and the neighbours. The system is therefore described by the plate capacitor formula $C = \epsilon_0 \epsilon_r \frac{A}{d}$. The system requires a thin oxide d with a large width $\sim A$ to maximize the coupling capacitance. On the other hand, the width $\sim A$ must not be too large to minimize the inter-strip capacitance and capacitance to the backplane. Of course, here also the strip pitch plays an important role. The minimum oxide thickness is limited by technological application and insulation robustness considerations. A standard choice of oxide thickness is around 200 nm. The strip designs also represent a geometrical deviation from a full plate capacitor to the backplane. The full depletion voltage of a strip array is greater than the one of planar diodes. Using the strip pitch p , strip width w for p^+ strips and w' for n^+ strips, and diode thickness d , the following relation is given in [17, 107] for double-sided sensors,

$$\frac{V_{FD}}{V_{FD0}} = 1 + \frac{2p}{d} \left[f_p \left(\frac{w}{p} \right) + f_n \left(\frac{w'}{p} \right) \right] \quad (1.39)$$

where V_{FD0} is the full depletion voltage for planar diodes and the functional forms f_p and f_n are given in [107]. This deviation has to be taken into account when $N_{eff} \propto V_{FD}$ is extracted from a segmented sensor instead of a diode. The total capacitance for the p-side strips can be expressed by [17]

$$C_{p-side} [\text{pF/cm}] \sim \left(0.75 + 1.8 \frac{w}{p} \right) \quad (1.40)$$

n^+ strips have larger capacitance than p^+ strips since the charge accumulated between n^+ strips makes the n^+ cathode effectively larger.

$$C_{n-side} [\text{pF/cm}] \sim 2 \left(1.5 + \frac{w'}{p} \right) \quad (1.41)$$

Besides the capacitance calculation, the detector design must take the potentials and resulting field configurations into account to guarantee a stable operation above the depletion voltage without any breakdown or micro-discharge. The Al strip implant configuration evolved over the last detector generations, going along with higher depletion voltages and potential configuration differences between single- and double-sided sensors. The breakdown field in intrinsic silicon is $V_{break} = \frac{\epsilon E_g^2}{2qN_{eff}} \approx 30 \text{ V}/\mu\text{m}$, defining the maximum field allowed before breakdown. This dictates at least some limits on the implant profile, which should be thick and round to avoid edge- or point-like structures with a high field, see Fig. 1.26a.

In the case of single-sided sensors, both the implant and Al strip can be at the same potential, most often GND. With double-sided sensors on one side, the implant to Al strip potential difference¹⁸ equals V_{bias} (see Fig. 1.26c), resulting in a strong fringe field at the edge of the strip. This results in micro-discharges caused by a large local field. The pure bias voltage is no longer the only field defining

¹⁸ Often split bias is used, where both coupling oxides carry $V_{bias}/2$ or the chip is kept floating.

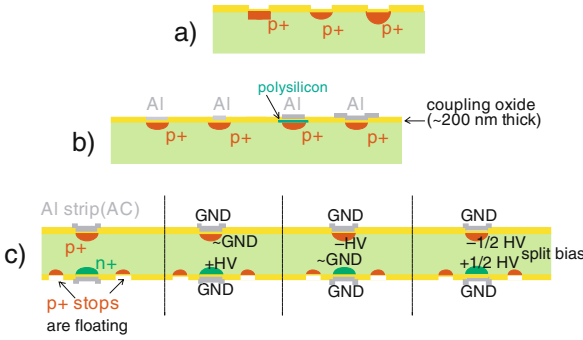


Fig. 1.26 Different strip designs. In first approximation, an AC-coupled sensor has a doped implant, a SiO_2 layer and an Al electrode connected to the readout. The common interest is to minimize the maximal E field at the pn-junction to avoid breakdown, by shaping the implant profile – avoid sharp edges and enlarge implant profile (this is demonstrated in part a). To increase coupling capacitance, the insulator oxide should be thin and Al and implant width large. Depending on the global sensor design and its operation environment, the strip layout has to be chosen very carefully to give the best possible field configuration. Double-sided sensors, having a voltage potential (see part c) between Al and implant, benefit from a narrower aluminium width with respect to implant. This ratio is very dependent on the needs, where a metal overhang is often sensitive to micro-discharge. In the single-sided CMS sensor, a large well-defined metal overhang was applied. With this configuration the electrical field is drawn partially into the SiO_2 , having a higher breakdown voltage. A deep implementation of an additional polysilicon layer inside the oxide also moves high field into the oxide (see right complex in b)

entity; (MOS effect). In addition to this, charge-up in the oxide, which comes with poor oxide quality, poor passivation or charge-up during radiation, also influences fields locally and can lead to local micro-discharge. To avoid the MOS and oxide charge effect the Al electrode on a double-sided sensor should be narrower than the implant underneath to reduce the electric field strength through the bulk in the vicinity of the implant strip edges, since the electrical field causes the undesirable micro-discharge, a precursor to breakdown of the junction. This leads to, for example, in the CDF II case, to a 14 (or 16) μm Al electrode with a 18 (or 22) μm implant for a sensor. Some possible configurations are displayed in Fig. 1.26b, where also an implementation of doped polysilicon into the oxide was tried to shift the highest field into the oxide with a 30 times higher breakdown voltage. The micro-discharge effect is described in detail in [129, 130]. Micro-discharge is a local problem, it also generates random pulse noise even before full breakdown. Figure 1.27 shows an example of current increase, localized in single strips at two different voltages. Of course the effects are all related to a high local field, which happen above V_{FD} .¹⁹ In a single-sided sensor, both aluminium strips and implants are at almost the same potential. The MOS effect is negligible and the Al electrode can be enlarged with respect to the implant to draw the high fields to the electrodes into the oxide. Another example of hand-tailored strip design is also described in [24, 32, 52, 53] and in Sect. 5.1.2 where the special needs of the CMS detector and its radiation tolerance

¹⁹ At least for p-in-n sensors, where the field builds up from the junction side.

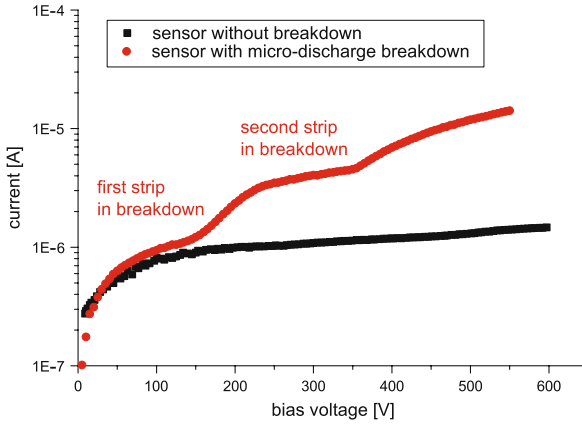


Fig. 1.27 An example of micro-discharge, the sensor shows a soft breakdown at a given voltage, the current increase is localized in a single strip

needs are explained. CMS uses a $4\text{--}8\text{ }\mu\text{m}$ metal overhang to draw the max field into the SiO_2 , refer to Fig 1.26b. In short, each new geometry needs to be carefully simulated to ensure proper operation without breakdown in the given environment, while respecting needs of good coupling to inter-strip capacitance correlation; the above discussion can serve as a guideline.

In addition to the discussion on micro-discharge and capacitance correlation, a broader metal strip width can also act as an electron repellent field plate with an applied potential on the n^+ -side instead of p^+ -stops (see Fig. 1.29 and 3.11).

Sensor Strip Capacitances

Three different components define the strip capacitance network. The basic design strategy is to maximize charge coupling towards the readout electronic avoiding parasitic capacitances and to minimize capacitance load, to ultimately reduce noise.

Coupling Capacitance (C_{coupling})

The coupling capacitance is measured between the implant and the aluminium read-out strip, which is directly connected to the readout electronics. Coupling capacitance should be large, being directly proportional to the signal. A large capacitance means a thin isolation layer between the implant and Al strip, which is difficult to achieve with a high reliability and without creating a short circuit between implant and readout strip, called a pinhole. Shorts or ohmic connections between Al and implant would violate the AC design, creating a DC coupling with a free bulk charge flow into the preamplifier. This limits the coupling capacitance to the manufacturing process reliability. DELPHI used integrated coupling capacitors, the value of $7\text{--}15\text{ pF/cm}$ was high enough with respect to the inter-strip and backplane capacity

of 1.5 and 0.2 pF/cm, respectively. Using dry and wet oxidation (see Sect. 1.8.2 on page 51), CDF increased the capacitance up to 140 pF per strip, a value of 20 pF/cm was specified for CDF to allow reliable production of two-layer capacitor dielectric (SiO_2 and Si_3N_4). With longer strips and broader metal strips CMS reached values between 300 and 600 pF depending on the sensor geometry, specifying $\frac{1 \text{ pF}}{\text{cm} \cdot \mu\text{m}}$. It has to be mentioned that reliable voltage resistant and thin, thus large, coupling capacitors were only technically realizable with additional nitrate layers.

Inter-strip Capacitance ($C_{\text{inter-strip}} = C_{\text{int}}$)

The inter-strip capacitance C_{int} is one of the major contributions to the capacitance load into the amplifier. It should have a certain value to share charge between two or more strips. Spatial resolution is increased by signals distributing charge on two or three strips, for one could calculate the “center of gravity”. Therefore good charge sharing between direct neighbours is desired. Sometimes additional intermediate strips are introduced to have a better charge sharing, without large effect on C_{int} . In order to get most of the signal into the preamplifier, the inter-strip capacitance should be much smaller than the coupling capacitance. These two restrictions lead to the specified value 1.0 pF/cm and the ratio $\frac{C_{\text{int}}}{C_{\text{coupling}}} = \frac{1.0}{20}$ for the CDF intermediate silicon layers sensors. This value is mainly determined by sensor layout and strip width to pitch ratio. For CMS the ratio stays between 1:30 and 1:60.

Backplane Capacitance (C_b)

To measure the strip to backplane capacitance, the measurement instrument has to be spanned from strip to backplane, while bias voltage is applied.²⁰ This is a major effort for high V_{bias} because the LCR instruments are restricted to lower voltages. In most cases C_b is approximated to $C_{\text{total}} / (\text{number of strips})$. But even without full or any bias voltage applied, the relative C_b measurement is an excellent identification tool for strip defects as there can be strip breaks, shorts between several strips and shorts to the implant.²¹ A broken strip shows a lower capacitance, but the capacitances of both strip ends sum up to the nominal value. Shorted strips come in pairs or groups; the capacitance will then be N times the nominal capacitance. Pinholes, short-circuit readout strip to implant, result in a very high increase of capacitance. The capacitance measurement of pinholes is highly frequency dependent and so a quasi-static instrument must be used. By measuring the values for every single strip, quality control can approximate the load uniformity of the preamplifier.

Strip Capacitance ($C_{\text{strip}} = C_d$)

$C_d = C_{\text{int}} + C_b$ includes all capacitances of a readout strip including inter-strip capacitances and strip to backplane capacitance. It reflects the total capacitance load

²⁰ Without full bias voltage, only the capacitance to the plane of the SCR would be measured.

²¹ Known as a “pinhole” (see Sect. 1.6.3).

to the chip amplifier. C_d is a major noise source of a silicon detector. CMS limits C_d to 1.2 pF/cm by defining width/pitch = $w/p = 0.2$, see Sect. 5.1.2.

Aluminium Resistivity (ρ_{Al})

There is a correlation between the resistance of the metal strip and the signal pulse shape imposing a minimum acceptable resistance. Resistance can be calculated from the width (w) and thickness (d) of the aluminium by

$$\rho_{Al} = \frac{2.824 \times 10^{-6} \Omega \text{cm}}{(d = 1.2 \mu\text{m})(w = 8 \mu\text{m})} \approx 30 \Omega/\text{cm} \quad (1.42)$$

and thus relates to the specifications of the metal strip width and thickness. While the width as discussed earlier is defined by other constraints, the remaining adaptable parameter is the thickness. The example calculation in formula (1.42) shows the specification of the CDF II ISL sensors, requesting a minimum thickness of 1.2 μm . The aluminium resistance determining the strip resistance acts as a series resistor for the readout electronics. For short peaking times, high ρ_{Al} significantly influences the noise (see Sect. 1.5).

Bias Resistors (R_{bias})

The bias voltage to the sensor is supplied through a set of polysilicon resistors $R_{bias} = R_{poly}$, connecting the implant strip to the bias ring, which is wire-bonded to the biasing terminal. Microscopic photos of polysilicon resistors are presented in Fig. 1.28. Noise contributions²² from the bias resistors are proportional to $\sqrt{\frac{kT}{R}}$, where k is the Boltzmann constant, T the temperature and R the bias resistor. This dependency imposes the requirement for a high value of bias resistance. Referring to formula 1.32 on page 27 the contribution is highly dependent on the readout frequency τ for experiments with long integration times, e.g. at LEP or ILC a high R_{bias} value is more important than for the LHC experiments. Variations of R_{bias}

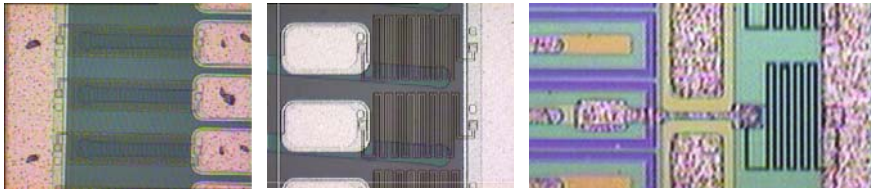


Fig. 1.28 A bias resistor made of polysilicon R_{poly} . The picture shows clearly the long and thin meander pattern of the polysilicon line, which ensures a high resistor value on a small area. The vias at the end of the polysilicon resistors to the p^+ strip as well as the vias to the bias ring are visible. Beneath the meander, the p^+ strip runs further to maximize the active area of the sensor. The pictures show a zoom of a CMS rectangular sensor, a CMS wedge sensor and a DELPHI n-side zoom

²² Thermal noise.

lead to voltage differences among individual strips and a non-uniform field distribution. Another upper limiting factor is the associated potential differences between neighbouring strips. Reliable polysilicon resistors with very high resistivity and only small deviations are difficult to process. The specification for the CDF II ISL sensors is $R_{bias} = 4.0\text{--}10\text{ M}\Omega$ with $\pm 10\%$ variation within a single sensor. For CMS a lower value is possible due to the operation temperature of -20°C , the specifications are $1.0\text{--}2.0\text{ M}\Omega$ with a maximum spread within one sensor of $0.3\text{ M}\Omega$. To measure the real bias resistor, the sensor has to be at least partially depleted to have the final field configuration on the strip side, isolating the individual strips; otherwise several resistors are measured in parallel, resulting in a lower resistance. Vice versa a low bias resistance, together with a higher leakage current is an indication for a low inter-strip resistance. The bias resistances are determined by measuring the voltage drop δV (V_x) over the resistor, with depletion voltage supplied, and the leakage current (I_L) through the sensor by short-circuiting the resistor with an ampere meter. The bias resistance is then calculated by

$$R_{bias} = \frac{V_x V_{bias}}{(V_x - V_{bias}) I_L} \quad (1.43)$$

with $V_{FD} = V_x + V_{diode}$ and $R_{sensor} = \frac{V_{bias}}{I_L}$.

In most quality assurance setups, a defined voltage V_{set} is imposed over the bias resistor, the current is measured and $R_{bias} = V_{set}/I_{measured}$ is calculated. Applying too high a voltage may disturb the fields, lowering inter-strip resistance and thus result too low measured R_{bias} values – CMS had to change the measurement voltage from 10 to 2 V. For irradiated sensors the single-strip current, in the same order as the imposed current, has to be taken into account.

$$R_{bias} = \frac{V_{set}}{I_{measured} - I_{strip}} \quad (1.44)$$

The polysilicon resistor processing is explained in Sect. 1.8.2, especially Fig. 1.43. In reality the company establishes the final design, the customer defines value and size. With an estimate on the value of the resistance/square,²³ a pre-meander structure can be designed.

To design a sensor, high values of R_{bias} are preferred for their low thermal noise, especially long ladders must have high value resistors because they all add up parallel, therefore the readout electronics sees a lower value and therefore higher noise. On the other hand large resistors increase the RC time constant. For highly irradiated sensors, the formerly very high (order of gigaohms) bulk resistivity drops and a good fraction of the applied voltage drops then on R_{poly} , an undesired effect, which would require a lower value. Here, R_{bias} also limits the strip current. With a high current, e.g. after radiation, R_{bias} defines the potential $V = RI$ of the implant with respect to the aluminium strip. This should be taken into account when designing the readout electronics.

²³ A square is a defined square size to allow normalization of a resistance per area.

Inter-Strip Resistance $R_{inter-strip} = R_{int}$

A high inter-strip resistance is necessary in order to accomplish the isolation of all individual strips. R_{int} should be in the order of several $G\Omega$. Obviously, this value is not applicable with doped silicon at non-cryogenic temperatures. It is only achievable with a fully depleted surface at the $Si-SiO_2$ interface reaching deep into the bulk volume. Inter-strip resistance is a very delicate parameter, sensitive to all kinds of oxide charge or even charge concentration in the passivation oxide spoiling the surface depletion to surface inversion or accumulation. Charge-up of the surface oxide will always affect R_{int} .

In Sect. 1.10.2, it is illustrated how radiation can decrease the inter-strip resistance ending up in values of several tens to hundreds of $M\Omega$. The most complicated part is the R_{int} measurement in the presence of bias resistors, in the order of several $M\Omega$, connecting all strips to the bias ring. This can be principally solved in applying a small voltage ramp on one implant strip (via the DC pad) and measuring the resulting current on the neighbouring DC pad, while both voltage supply and amperemeter share the same ground, namely the bias ring. Unfortunately only a small voltage on the order of about 1 V can be applied without disturbing the depletion layer configuration, thus short circuiting the strips. Applying 1 V over a resistance of $1 G\Omega$, the resulting current of 1 nA is in the order of the leakage current. With resistance values of 10–100 $G\Omega$ or high strip leakage current, e.g. after irradiation, the measurement current cannot be resolved any more, therefore the method can only give a lower limit for R_{int} .

n-side Isolation

Keeping in mind the band structure on the *n*-side, positive fixed oxide charge on the $Si-SiO_2$ attracts a layer of mobile electrons. Without additional precautions, *n*+strips would be short-circuited by this electron accumulation layer. Isolation is achieved via implantation of p^+ (p^+ stops) surrounding each *n*+ strip with an individual or “atoll” configuration. The additional p^+ implants are necessary to dissipate the electron accumulation layer at the $Si-SiO_2$ boundary. The aim is to cover as much area as possible of the gap between strips without actually contacting the strips. The yield should not be lowered by coming too close. Another possibility would be the p^+ spray technology, where a diffuse layer of p -dopants is introduced. Often a combination of both p^+ stops and p^+ spray techniques are used. These isolation designs are necessary features for *n*-in-*p* sensors under investigation for future detectors, like at the SLHC. Another way to repel the electrons is to increase the Al strip widths, apply a potential and use them as “field plates”. In Fig. 1.29 the different isolation methods, namely p^+ stop, p^+ spray and a combination of both are schematically drawn.

Examples of application are to be found in Fig. 3.11 and a photo of p^+ stops can be visited in Figs. 3.10 and 4.19, a schematic can be found in Fig. 4.18.

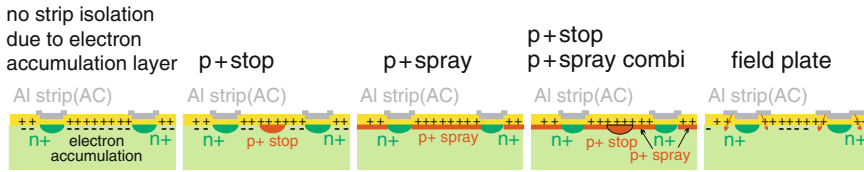


Fig. 1.29 Positive charges in the oxide attract electrons in the n-bulk material to the interface where an electron accumulation layer forms and short-circuits the strips. The basic mechanism to avoid this is to repel the electrons by the introduction of p+ dopant in an isolated region or simply distributed/sprayed in the inter-strip zone. These methods are called p+ stop, p+ spray or a combination of both. A fourth method is the use of a metal overhang of the AC pad at slightly negative potential to repel the electrons (A more detailed discussion about the Si-SiO₂ interface can be found in Sect. 1.1.3)

Strip Faults

The most common strip faults are introduced, together with a measurement example and their effect on the readout electronics. There is always a compromise of defective strip percentage e.g. in CMS it was 1% to have a maximum of 2% bad strips on a two-sensor module. Long modules, with 10 sensors daisy-chained, need a much stricter criterion and vice versa a very simple and standard sensor design. A specified request of zero strip faults would decrease the numbers of accepted sensors, thus the yield. This would result in substantially higher cost. In the case of the daisy-chaining of several sensors, the sensor containing a strip fault should be placed as far from the readout hybrid as possible. This is especially true for breaks and pinholes, where the strip should be disconnected. The basic faults are illustrated in Fig. 1.30 as well as photos of shorts and breaks.

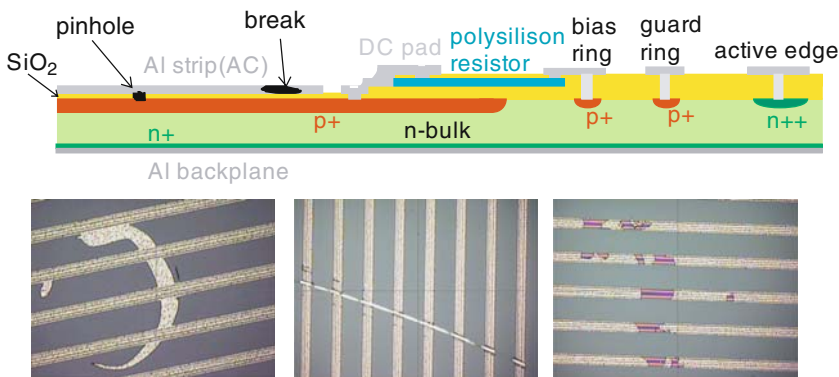


Fig. 1.30 The location of pinholes and breaks are shown in the sensor scheme. Shorts are displayed in the first two photos, where one results from a processing fault, whereas the second came from wrong handling. The breaks are simple process faults, but are often also results from scratches

Pinholes

Pinholes are shorts or low ohmic connections between an aluminium readout strip and implant. Charge can flow freely into the preamplifier, overloading the amplifiers of the main part of one whole chip (refer to [78] and [83]). These strips must be identified if not avoided in the manufacturing process and remain disconnected from the amplifier. Commonly the following strategies are used to identify pinholes:

- applying several volts over the insulation between Al readout strip (AC pad) and the implant (DC pad). Simultaneous measurement of the current identifies all shorts and measures the resistance of low ohmic connections. Pinhole signatures are mA signals on a sub pA background for good strips.
- high $C_{coupling}$ hints the presence of a pinhole but for an LCR device $C_{coupling}$ measurement is also frequency dependent. With quasi-static devices,²⁴ measuring $Q = CV$ in steps, $C_{coupling}$ is out of range for pinholes.
- strip to backplane capacitance C_{back} also identifies pinholes quite easily. In this case the operation voltage is applied via the LCR metre, which cannot stand high voltages. Of course, a decoupling box could be applied but then the above-mentioned methods are as effective and easier. Therefore, the method is only easily applicable for low depleting sensors.

Finally in case of a pinhole, the wire connection between strip and preamplifier has to be pulled. In the case of the SVX4²⁵ chip, single channels can be even disconnected later, when configuring on chip level (refer page 62).

Breaks

Breaks are no danger to the readout, but will disconnect the rest of the strip and therefore all strips of the next sensors in a line. Sensors with breaks should be placed at the end of the ladder (like pinholes). Breaks are identified by comparing the current strip capacitance with the nominal strip capacitance. Strips with lower capacitance are candidates for breaks. For the DELPHI sensors, the capacitances of both strip ends were measured, where sum of the two values equals the nominal capacitance $C_{left} + C_{right} = C_{nominal}$. If the sum is equal to the nominal value the aluminium strip is broken.

Shorts

A short is given by a connection of one or more neighbouring strips. This is not a crucial fault, but will result in a higher load capacitance which associates a higher noise and also generate multistrip hits, degrading the resolution. This kind of fault

²⁴ A quasi-static capacitance measurement, where $Q = CV$ is measured for several values of V , works only with negligible current. In the case of a pinhole, the applied voltage V initiates a current driving the measurement value into overflow – pinhole signature.

²⁵ The SVX4, the successor of the CDF SVX3 chip.

has no preferred position in the sensor row. Shorts are found by measuring C_{strip} . Capacitances which are N times the nominal capacitance should come in groups of N members. $C_{strip} = N \times C_{nominal}$ for N strips shorted together.

Leaky Strips

Strips with a high leakage current can increase the channel noise dramatically. In combination with a pinhole, a not so rare case, the current can even overload the whole chip. There are many reasons for leaky strips, e.g. defect bias resistors, inhomogeneity in the bulk silicon especially in the surface region, faulty strip implantation, non-depleted regions, etc. (refer Sect. 1.13). These strips often come in groups, which means a whole region has some defect. Very high currents increase the shot noise. In some cases, leaky strips even have a stochastic time structure, e.g. resulting from micro-discharge and therefore can produce noise deviating from standard shot noise. During quality control leakage current will always be measured at the maximum operation voltage, e.g. 80 V for CDF or 400 V for CMS; high current average or localized outliers are critical. Some examples of high strip leakage currents are presented in Sect. 1.13.

1.7 Practical Aspects of Handling and Testing Silicon Strip Devices

One reason to use silicon sensors is their robustness. SiO_2 -passivated silicon sensors are impervious to their environment in some well-defined boundaries. Sensors do not degrade even after resting in cupboards for years. A clean room is sufficient for sensor testing and module assembly; no dedicated rated cleanroom of better than class 100 000 is necessary.

On the other hand sensors are thin, brittle and fragile. The passivation layer is only around 1–2 μm thick and provides almost no protection against mechanical damage. Scratches from bad handling or heavy dust during transportation degrade sensor properties, refer to Sect. 1.13. Also probe needles with probe tips around 2–7 μm need to touch the aluminium pads and the risk of damaging the pad or even to pierce through the metal is not negligible. Sensors need to be handled with care and some healthy paranoia not to destroy them. Vacuum tweezers are standard tools to avoid any direct human contact. The cleanliness of the sensor surface is also very important for the latter wire-bonding. Remnants, e.g. fat from a human fingerprint, can already significantly degrade bondability. Humidity levels in the laboratories have to be in well-defined ranges; very low humidity increases the risk of static electrical discharge and also charge-up of the sensors; a high relative humidity level ($> 30\%$) can lead to increase of leakage current, as silicon is hygroscopic. A standard method is to allow a normal humidity (40–50%) in the laboratory while sensors are stored in a dry cabinet and sensor probe stations are flushed with dry air during

testing. Charge-up of the passivation oxide can affect the $Si-SiO_2$ interface layer, refer to Sect. 1.13.

There are some dependencies, which can be explained more by “10-years-gut-feeling” and experience rather than by some mathematical formulas.

- sensors have to be stored in a dry and dark environment
- sensors have to be handled with vacuum tweezers
- face masks have to be worn, the human breath contains some acids, which can degrade sensor performance
- sensors are tested under low relative humidity ($< 30-40\%$ RH)
- testing should be one’s second nature but a certain paranoia helps to prevent stupid faults out of carelessness
- if a measurement looks “strange” repeat it; sometimes the sensor needs to be conditioned, e.g. some charge-up has to be drained off
- most often electrical defects are reflected in optical defects
- strange results often reflect wrong measurement parameters, e.g. too high voltage deteriorating surface depletion for inter-strip resistance measurement (Sect. 1.1.3)
- bad contacts are often related to insufficient opening of the aluminium pads and remains of SiO_2 are good insulators. In this case bonding also becomes more difficult
- a stabilized temperature is mandatory for measurements of irradiated sensors to
 - get reasonable, understandable and comparable results
 - avoid thermal runaway, which may even destroy the sensor
 - measure the α parameter (see Sect. 1.10.1), which is strongly temperature dependent

1.7.1 What is the Standard/Exhaustive Set of Quality Assurance Tests?

Sensors for HEP detectors are procured from industry. The quality assurance by the producer is by standard quite strict and part of the contract. A strip yield above 98–99% is a standard requirement. Furthermore, maximum leakage current and a range for the depletion voltage is requested. In addition all the above-discussed strip parameters, like inter-strip capacitance, inter-strip resistance, bias resistance and coupling capacitances are specified. Furthermore more process-related parameters, like flat-band voltage, breakdown voltage, aluminium resistivity dielectric breakdown voltage, etc. are specified. Process parameters are definitively only tested on sample basis and mostly on dedicated structures.

Depending on the number of sensors, sample testing is appropriate after pre-production is sufficiently evaluated. But without full testing, there is always the chance, assembling several sensors plus hybrid together, to spoil the whole module.

The minimum tests are

- global current–voltage characteristic (IV)
- full capacitance–voltage ramps (CV) to determine depletion voltage

Quality Assurance on Sensor Level

For strip testing, there are different more or less exhaustive strategies but some standard sets of tests are

- global tests:
 - IV scan ($0-V_{IVmax}$), where $V_{IVmax}(\text{CDF}) = 100 \text{ V}$ and $V_{IVmax}(\text{CMS}) = 550 \text{ V}$ (or 800 V)
 - CV scan ($0-V_{CVmax}$), where $V_{CVmax}(\text{CDF}) = 100 \text{ V}$ and $V_{CVmax}(\text{CMS}) = 350 \text{ V}$
- common strip tests:
 - leakage current of each strip at V_{strip} (to determine noisy, leaky strips), where $V_{strip}(\text{CDF}) = 80 \text{ V}$ and $V_{strip}(\text{CMS}) = 400 \text{ V}$
 - bias resistance of each strip (R_{poly})
 - I_{diel} current over C_{AC} , where $V_{diel}(\text{CDF}) = 60 \text{ V}$ and $V_{diel}(\text{CMS}) = 10 \text{ V}$ to identify pinholes
 - coupling capacitance $C_{coupling}$ with quasi-static C-metre or low LCR frequency ($\sim 100 \text{ Hz}$)
- measurements on sample, problem basis or on dedicated structures
 - inter-strip resistance
 - inter-strip capacitance at high LCR frequency ($\sim 1 \text{ MHz}$)

To guarantee the quality, every single strip has to be tested to identify the percentage of bad strips. For double-sided sensors, all tests have to be done on both sides.

Process Monitoring

Until the CMS experiment, process parameters were checked on first prototypes together with the producer or not at all. For the 24328 sensors of CMS, a new concept was developed to allow an easy measurement of silicon device parameters and to efficiently monitor the production process [25, 105]. A set of test structures was designed and placed on every wafer for all sensor types. Figure 1.31 shows the cutoff from a 6 in. wafer with the test structures. These test structures also allow destructive tests to be done, like breakdown voltage of the coupling capacitors. A proposed set



Fig. 1.31 Half-moon with test structures. *Left to right*, the structures with the following accessible process parameter are located (1) TS-CAP ($C_{coupling}$, V_{break}), (2) sheet (Resistivity_{Al}, Resistivity_{p+}, R_{poly}), (3) Gate Controlled Diode (GCD) ($I_{surface}$), (4) CAP-TS-AC ($C_{inter-strip}$), (5) full minisensor, (6) CAP-TS-DC ($R_{inter-strip}$), (7) Diode (V_{FD}), (8) MOS1 ($V_{flat-band}$), (9) MOS2 ($V_{flat-band}$)

of measurements is leakage current and breakdown voltage measurement plus determination of depletion voltage on a minisensor comparable to the main sensor plus tests on standard diodes. Flat-band voltage and surface currents can be extracted on MOS and special structures called *Gate Controlled Diodes* (GCD). Inter-strip parameters like resistance and capacitance plus aluminium and implant resistivity and bias resistance can be taken from individual dedicated structures. Of course, this effort is reasonable, if the measurements and analysis are fully automated. An example of parameter evolution vs. time can be regarded in Fig. 1.74.

Irradiation Quality Control

With radiation becoming more and more an issue for today's and future detectors in a collider experiment, radiation hardness studies are more and more important. For CMS a dedicated radiation hardness quality control concept was set in motion to irradiate around 5% of the above-described test structures plus about 0.5% of the received sensors and even a couple of fully assembled modules. Proposals for pre and post radiation tests at nominal operation temperature on sensors and minisensors are

- mandatory tests on sensors
 - IV and CV (determine V_{FD} and compare with model)
 - inter-strip capacitance and resistance
- additional measurements
 - coupling capacitance
 - bias resistance
 - strip leakage currents
- measurements on modules
 - noise
 - signal to noise

Unlike sensor quality control, measurement of all strips is not necessary, the difference of pre and post radiation values are important. To get an even deeper understanding, all parameters, also strip parameters, are measured for several bias voltage values to better understand the behaviour below and above depletion voltage. After irradiation often over-depletion is even more important than before. The CMS irradiation quality control example is described in detail in [56, 67].

1.8 Production of Silicon Sensors

The basic material for the manufacturers of silicon sensors is sand SiO_2 quartzite, existing in abundance. It is cheap, the price of a sensor is completely driven by the number of processing steps and the required quality. The success of the different companies is due to a deep understanding of the different processes and required

recipes. The basic principles are known to everybody but the tiny details are always “company secrets”. The subject of silicon processing could easily fill a unique book. The next sections focus on the following steps:

- silicon crystal (“ingot”) production
- slicing into wafers, lapping, etching and polishing wafer
- processing
 - oxidation
 - photolithography in between almost all the steps
 - doping by ion implantation
 - annealing
 - metallization
- dicing (cutting) the sensor out of a wafer
- testing

This sequence grandly simplifies the real process with nearly 60 to 100 steps, e.g. some additional annealing for re-diffusion of previously introduced dopants or removal of defects. In addition, in between each major step there are extensive cleaning cycles, lots of acidic chemicals as agents are used as well as very pure de-ionized water.

1.8.1 From Pure Sand to Detector Grade Silicon

The starting material is simple mined quartz sand (SiO_2), undergoing extensive purification and distillation. The first step is to produce *metallurgical grade silicon*, 95–99% pure silicon (MG-Si) in a series of melting processes at temperatures from 1500 to 2000°C, while applying carbon in the form of coke or coal. The oxygen then combines to carbon monoxide, leaving chips of MG-Si ($\text{SiO}_2 + 3\text{C} \rightarrow \text{SiC} + 2\text{CO}$ then $2\text{SiC} + \text{SiO}_2 \rightarrow 3\text{Si} + 2\text{CO}$ at temperatures around 1500–2000°C).

In the next purifying step MG-Si is subjected to HCl in a fluidized-bed reactor to form trichlorsilane ($\text{Si} + 3\text{HCl} \rightarrow \text{SiHCl}_3 + \text{H}_2$ at temperatures around 300°C); in this course many impurities are removed. The next purification step to accomplish an impurity concentration of less than 1 ppba²⁶ is achieved by distillation.

The hyper-pure SiHCl_3 conversion to hyper-pure silicon is finally accomplished by Chemical Vapour Deposition (CVD), where SiHCl_3 is vapourized with highly pure hydrogen additive in a deposition reactor ($\text{SiHCl}_3 + \text{H}_2 \rightarrow \text{Si} + 3\text{HCl}$ at temperatures around 900–1100°C). The final silicon then slowly grows on ~1000°C hot slimrods in a few days to *Electronic Grade Silicon* (EGS) and has achieved the commonly known “eleven nines” (99.99999999%) <1/100 ppb purity. The slimrods are then broken to pieces, dopants are added and the whole melange heated up to a melt in a quartz crucible. The real processing starts by growing a single crystal ingot from the polysilicon including the needed dopant additive. The most common

²⁶ 1-ppba: part per billion active (impurities).

method of wafer development is the Czochralski (“Cz”) growth: The silicon melt is held just a few degrees above the melting point and a single rotating crystal as seed initiates the growth at the top. The slow retraction allows the melt to solidify in perfect crystal orientation at the boundary. The growth is controlled by the pull rate, the melt temperature and the rotation. Intrinsically for this method, oxygen dissolves into the melt during the process, enriching the final crystal homogeneously with oxygen.

The second method is the *Float Zone Crystal* technique (“FZ”), where a polysilicon rod is brought into contact with a seed crystal and the rod is then locally melted with RF heating. The RF heater and therefore the melted zone moves along the rod. The impurities have a different diffusion constant and tend to stay in the liquid, leaving a pure single crystal. The ingot growing apparatuses of the FZ and CZ techniques are displayed in Fig. 1.32. In addition the silicon rod has *no* contact to any melt or crucible.

The typical length of a single crystal ingot is 1–2 m. The ingots are normally not fully round and are then grinded to real cylinders, also a flat or a notch is applied to indicate the crystal orientation.

For several years the FZ technique was superior to the CZ method with respect to purity (e.g. oxygen content) and was therefore the only possibility to achieve “sensor grade” silicon. Also high resistivity material was not available due to the lack of commercial applications. With a better purity and therefore a longer charge carrier lifetime it was also the preferred material for solar cells. Nowadays, the CZ also realizes “sensor grade” material and probably the high oxygen content makes it interesting for the SLHC project, see Sect. 6.1.

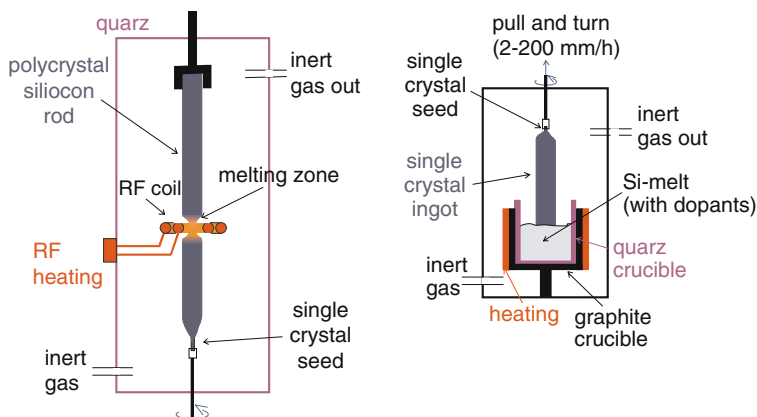


Fig. 1.32 The left picture shows the *Float Zone* method (FZ), where a polycrystalline silicon cylinder from a mold with a single crystal seed on one edge is subjected to RF heating, melting the cylinder to form a single crystal or “*ingot*”. The impurities have a higher solubility, therefore impurities diffuse to the boundaries further purifying the crystal.

The right picture shows the *Czochralski* method (CZ), where the single crystal “*ingot*” is directly drawn out of the melt using a single crystal as seed. The *Czochralski* method is most common globally, it additionally allows easy adding of dopants directly into the melt



Fig. 1.33 A silicon ingot, source of about 200 wafers. The picture shows raw silicon chips, a full size silicon ingot and sliced silicon wafers of different size. [Copyright Sitronic AG]

The silicon ingot now needs to be cut into thin disks, called “wafers”. The actual thickness is still not final but already below 1 mm. The cutting is achieved by a disk with a diamond blade or for multiply synchronous dicing a *Multi Wire Saw (MWS)*, where diamond-coated wires are arranged in parallel to cut several disks at once. The sliced wafers have to be cleaned before processing, which is achieved by

- lapping: grinding away large imperfections, also wafer edges are shaped
- etching “chemical polishing”: full removal of imperfections, micro-protrusions and surface impurities, wafers in special chemicals are agitated, rinsed, heated, dried, like porcelain dishes in a home dishwasher
- polishing: final polish²⁷ is needed to ensure a minimum number of defects and guarantee the specified thickness pieces of silicon, an ingot and cut wafers are shown in Fig. 1.33.

1.8.2 Processing

The processing steps are not different from standard integrated circuit chip processing (memory chips, processors). The photolithography step, explained just once, happens basically in between all further steps. As an initial step, a high resistivity polished silicon wafer (1–10 kΩcm) is covered with SiO_2 .

Silicon oxide growth is a key process step in the manufacture of all silicon devices. Outer layers of silicon wafers in a heated quartz tube, a furnace (see Figs. 1.34 and 1.35), are transformed to SiO_2 by an atmosphere of O_2 , H_2O steam or N_2O . In the “dry” process, pure dry oxygen is employed, the oxide grows very slowly realizing very uniform layers with high quality and few defects at the oxide–silicon

²⁷ To process a double-sided sensor, the wafer needs to be polished on both sides. This step, as easy as it sounds, is not available on both sides from all manufacturers.

Oxidation in dedicated furnace

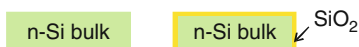


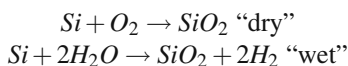
Fig. 1.34 Silicon oxidation: to enable segmentation and structuring, the raw silicon wafer is first subjected to an oxygen or water atmosphere at 800–1200°C in a furnace (*see* Fig. 1.35). The wafer is afterwards fully embedded in a SiO_2 layer



Fig. 1.35 Two quartz tubes in the furnace are visible on the *left* photo including the loader of several wafers. Each individual furnace has a well-defined atmosphere and always remains at the same temperature and content mixture. There is one furnace for each individual process. On the *right*, several burning furnaces are shown. Courtesy of ITE Warsaw [156]

interface. This process is mostly used for dielectrics for coupling capacitances ($\sim 100\text{--}200\text{ nm}$) of AC-coupled sensors and for MOS ($\sim 100\text{ \AA}$) transistors.

In the “wet” process, H_2O steam is injected, the oxide grows fast. The additional hydrogen atoms may degrade the oxide quality, the process is mostly used for thick field oxide or maybe passivation oxide ($\sim \mu\text{m}$). The processes are



For SiO_2 used as insulator, e.g. in between metal layers, SiO_2 obviously cannot be grown, in these cases sputtering is used – deposited oxide.

Figure 1.36 describes the photolithography and etching process. First, for each layer, a mask²⁸ is needed, which is normally a chromium pattern on a glass plate.

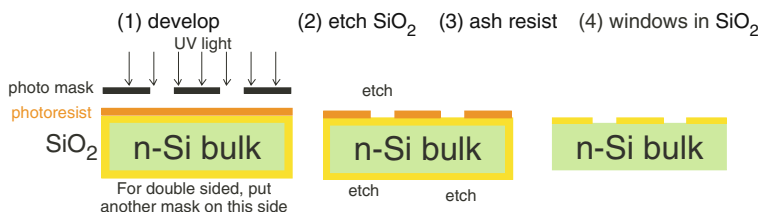


Fig. 1.36 First segmentation step: The oxidized wafer is now covered with photoresist, parts of the resist is then masked and subjected to UV light; after final development, the sensor is etched. As a final step the resist is etched away leaving defined windows in the SiO_2 layer

²⁸ The mask itself is very expensive.



Fig. 1.37 Photoresist is roughly spilled in the middle of the wafer, centrifugal forces, during fast rotation, homogeneously distributes the resist on the wafer. Courtesy of ITE Warsaw [156]

Then, the wafer is covered with UV light-sensitive photoresist, which is spilled on the fast rotating wafer in the spinner (see Fig. 1.37). UV light exposure of the resist through the mask transfers the patterns to the wafer. A final development step, like in every photo studio, is also necessary. Figure 1.38 shows a picture of the mask-aligner and the spinner, this part of the clean room area needs to be especially clean. Any dust particle during lithography will end up as a sensor defect later. Additionally, in some cases, the photoresist undergoes a heating cycle for hardening purpose to make it more resilient for different processing steps.

The pattern allows a controlled removal/etching of SiO_2 on the sensor to enable a controlled implantation later, the SiO_2 serves as a screener.

There are two basic etching methods:

- **wet etching** uses liquid etchants, where wafers are immersed in the solution. Wet etches are selective, isotropic and fast. Time, concentration and applied temperature of the immersion are important. Also crystal orientation has to be taken into

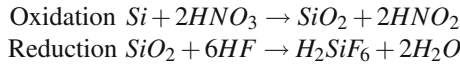


Fig. 1.38 On the left the mask-aligner is printing the mask onto the photoresist with UV light, opening the windows for the next etch process step. On the right, the spinner and developing machine can be seen. Courtesy of ITE Warsaw [156]

account, e.g. $\langle 100 \rangle$ *Si* can be etched 100 times faster than $\langle 111 \rangle$ *Si*. Wet etching is also used for SiO_2 , silicon nitride, polysilicon, photoresist, etc.

- **dry or plasma etching** uses gas phase etchants in a plasma. Directional etching is possible by applying electrical fields to direct ionic species in the plasma, there are reactive and ionic components. The etching is also very selective. Plasma etching stresses the object and needs an annealing step at higher temperature afterwards, it is therefore not applicable after metallization.

In Fig. 1.39 both plasma and wet etching laboratories are shown. The full etching recipes are always adapted to the dedicated device and are an important know-how of the manufacturer. Basically *Si* is etched in a two-step process



while etching of SiO_2 is a one step process



Aluminium etches in water, phosphoric, nitric and acetic acid mixtures.

And finally the photoresist has to resist all the above etchants to serve as a mask. After the etching, the remaining resist will be etched away, last portions of the resist will be dissolved by oxygen or fluorine plasma, mostly this goes along with an other wet cleaning step. In the next step the strip implants or homogeneous back-planes are realized by ion implanting or diffusion. An older version of an ion implanter can be seen in Fig. 1.40. A couple of patterned wafers are placed in a rotating disk to guarantee a homogeneous irradiation. Ions are then accelerated towards the wafer and are finally implanted, e.g. a 15 keV B^+ beam results in a low doping with about $N_{\text{acceptors}} \approx 5 \cdot 10^{16}/\text{cm}^2$ or a 30 keV As^+ beam for a deeper doping with $N_{\text{donors}} \approx 5 \cdot 10^{15}/\text{cm}^2$. Doping penetration for energies below 300 keV stays well below 1 μm . The SiO_2 or photoresist acts as a mask. The standard example,



Fig. 1.39 On the *left*, the plasma etching laboratory of a silicon plant in an institute is shown. On the *right*, the wet etching facility is displayed. The secret and art lies in the special recipes to use the right acid, the right duration and time on the different structures and materials, like Si, SiO_2 and Al. Courtesy of ITE Warsaw [156]



Fig. 1.40 The picture shows an ion implanter. Ions are accelerated and guided onto the target inside the sphere, where several wafers are rotated and homogeneously hit. The ions do not penetrate through the masking layer (SiO_2 or photoresist), therefore well-defined patterns, e.g. strips/pixel can be implemented on the wafer. Courtesy of ITE Warsaw [119, 156]

also cartooned in Fig. 1.41, is the implantation of small $p+$ lines into the n silicon bulk, creating many local pn -junctions – the strip and ring pattern. After an implantation, a high-temperature step is necessary to anneal structural damages. The ion implantation results in a very shallow doping. The temperature treatment also stimulates dopant diffusion and drives dopants further into the volume and smoothes edges. Full plane doping, like the backside, is often realized via diffusion. Diffusion dopant sources can be gases, doped amorphous silicon or dopant-enriched glasses, like boron or phosphoric glasses, which are deposited on the surface and etched away after the diffusion process. During one side processing the other side is protected by a SiO_2 layer.

For an AC-coupled sensor, several steps are needed to build high-quality thermal grown oxide, where the basic steps are shown in Fig. 1.42. The full wafer again undergoes one to several high-temperature steps in the oven with steam, oxygen or nitrogen atmosphere to achieve sophisticated, thin and voltage-stable oxide; sometimes also layers of polyimide are applied. The result is a thin isolating oxide

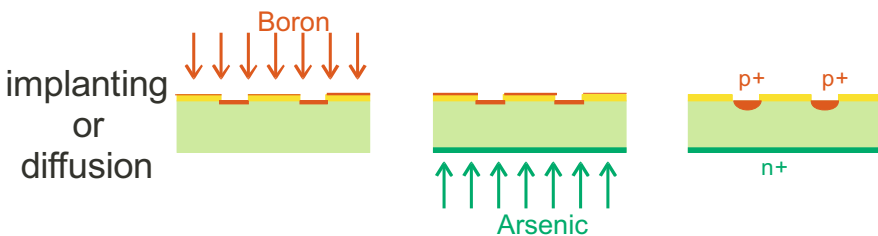


Fig. 1.41 Ion implantation or diffusion is utilized to realize the pn -junction with B on the front side and avoid a Schottky contact on the backside with As. SiO_2 is used as a mask

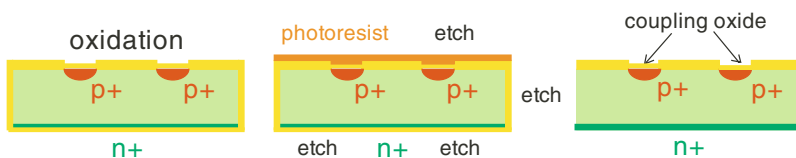


Fig. 1.42 To capacitively isolate the $p+$ from the aluminium readout strip, a layer of high-quality SiO_2 is introduced by thermal growth. As for all thermal oxidation the oxidation is applied to the full wafer. A photoresist step on the front and an etching step is needed to allow backside oxide removal. In most real structures, patterns of silicon oxide and silicon nitride are applied for the strip pattern

above the strips and thicker oxide in the strip intermediate areas. Quite often additional oxide deposition is applied beneath the final pads for micro-bonding to increase thickness and strengthen the structures. To remove the oxide from the back, photoresist is spilled on the front without mask, and the back oxide is etched away.

For the basic strip concept all steps but the final metallization and passivation are described so far. Besides the strip and ring structure processing, several additional steps are needed to apply the bias to the $p+$ strips. The most complicated and most common case, the polysilicon resistor biasing, is introduced briefly in Fig. 1.43.

Finally the back side will be fully metallized for simple electrical contact, while the front side must be patterned and needs additional steps (Figs. 1.44 and 1.45). For metallization, most often aluminium is used, due to its good electrical conductivity ($\approx 3.7 \cdot 10^7 \text{ S/m}$), its good connectivity to silicon and finally its easy shaping by photolithography. Aluminium coverage is achieved by chemical vapour deposition (CVD) sputtering process. For the front side another lithography step deposits photoresist, in a later development step windows are opened and aluminium is etched away. Additionally, there are a lot of testing steps in between all these processes to guarantee quality and to fully identify problems early in the process chain.

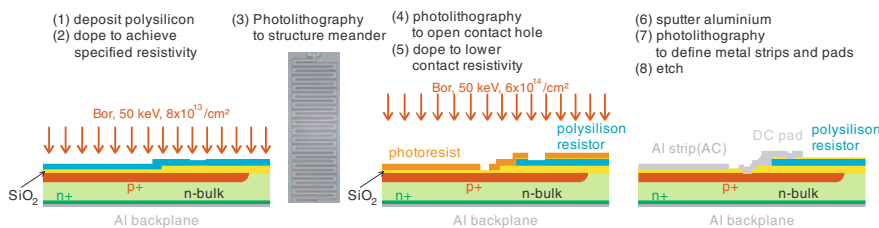


Fig. 1.43 The request of a polysilicon biasing comes along with several additional process steps. First, the sensor is fully oxidized and then covered with a CVD-deposited layer of polysilicon. Resistivity is defined by a controlled doping by ion implanting, with, e.g. boron. As done initially, the wafer is oxidized, structured by a lithography process where only the final bias meander is covered with photoresist, and most of the poly is etched away. The absolute resistance is now defined by initial resistivity, length and width of the polysilicon resistor. Another lithography step is needed to open small windows for the metal contact to lower the contact resistivity of the polysilicon locally. Final opening of the contacts into the oxide to the $p+$ -strips, the poly meander and the bias ring allows final metallization. The cartoon is presented as a side view of the sensor

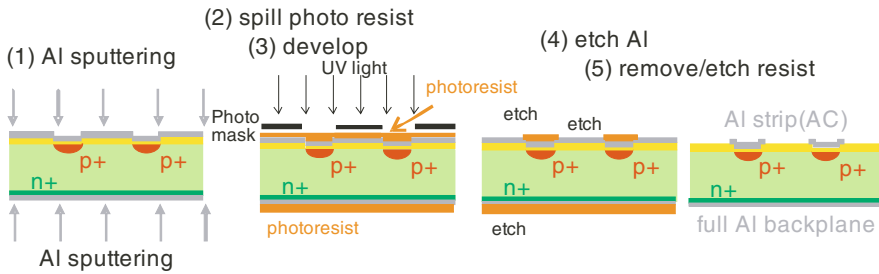


Fig. 1.44 As for the oxide, the full surface is metallized by a CVD sputtering process. Another lithography and etching step later, aluminium strips, pads and rings are formed. For a good electrical contact, the back side is fully covered with aluminium

At this stage, a single-sided DC-coupled sensor is completely processed waiting for its final cleaning, passivating and cutting step. For the second face, the ohmic side processing, only the combined layer processes are briefly described; the detailed steps, like lithography and etchings, etc., are the same as for the junction side and are not elaborated in detail. The different steps are illustrated in Fig. 1.46. One of the complications is the necessary protection of the other side. Double-sided sensor processing is only possible on substrates that are polished on both sides. A strip-like segmented $n+$ layer replaces the formerly described full area $n+$ implantation. To establish strip isolation additional $p+$ stops are needed. And finally, aluminium lines are needed on top of the $n+$ strip above the coupling oxide, as well as all pads, bias and guard rings.

In a lot of cases, the processing does not end here. Another isolation layer (of SiO_2 or polyimide) is needed, pierced by vias, connecting to aluminium routing strips above the isolation.

In principle none of the above-described steps are problematic if isolated. In the full combination with the necessary purities, one has to fear pinholes, failed vias, increased capacitance, cross talk between channels, tiny contamination in some oxide layers, failures affecting neighbour or other side strips, etc. Keep in mind that different from standard chips, one single sensor covers the **full** wafer, therefore one

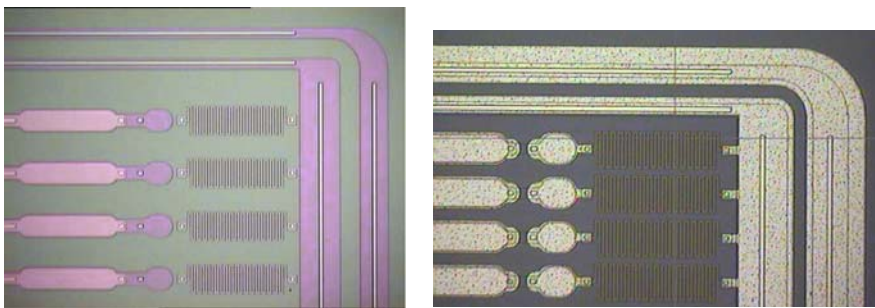


Fig. 1.45 The *left* shows all the $p+$ structures and polysilicon resistors before the final aluminium is applied in comparison to the final step on the *right*. An interesting feature of the guard and bias ring to mention here is the *continuous* via contact from the final aluminium layer to the $p+$ -layer underneath

- (0) Initial situation: strip implants ready (p-side protected)
- | | | |
|-------------------------------|-----------------------------|----------------------------------|
| (1) open windows for p+ stops | (2) add p+ stops | (4) apply aluminium (both sides) |
| (a) spill resist | (a) implanting or diffusion | (a) sputter aluminium |
| (b) apply mask, UV | (b) anneal (heat) | (b) spill resist |
| (c) develop | (3) apply oxide | (c) apply mask, UV |
| (d) etch window | | (d) develop |
| (e) remove resist | | (e) etch non-strip region |
| | | (f) remove resist |

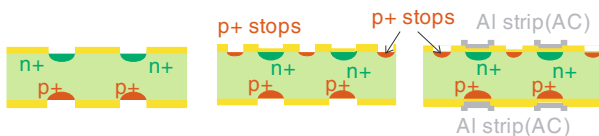


Fig. 1.46 The cartoon illustrates the many additional steps needed to structure the ohmic side. $n+$ strip segmentation on the ohmic is implemented analog to the $p+$ strips technique on the junction side described earlier. Additional $p+$ stops necessary for $n+$ strip isolation also need lithography, implantation and annealing steps analog to the strip processing. Coupling oxide is applied via thermal growth (this step is not illustrated). Finally on top of the $n+$ strips aluminium strips are formed

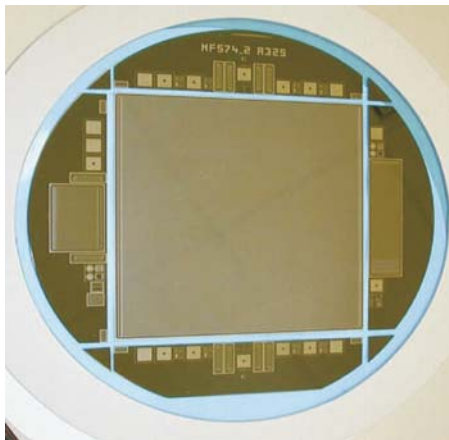
single defect may be enough to reject a processed whole wafer. Finally the full wafer is passivated most often with a rough layer of sputtered SiO_2 but also commonly with polyimide. The passivation is for protection, otherwise silicon would react with all contaminants in the environment. A last etching step is required to make the required metal pads accessible for micro-bonding (see Fig. 1.11), of course another mask step is needed.

Sensors and chips are always processed on the full wafer, the last step before testing and packaging is the precision cutting of the sensor out of the wafer, see Figs. 1.47 and 1.48. Sensor or chip cutting is normally done by a diamond saw and continuous water flushing. Experience tells that even for experienced companies, breaks and burns are common. Meticulous optical checking during quality assurance



Fig. 1.47 The cutting of chips with a diamond saw. Note the high water flux to avoid heating up due to the high rotation speed. Courtesy of ITE Warsaw [156]

Fig. 1.48 A CMS sensor cut from its wafer. The blue foil, the wafer rests on, was not cut



is very important. To have more complicated cuts than straight lines, laser cutting is the state of the art, used for LHCb²⁹ sensors.

An example summary of all main process steps needed to process a double sided sensor is shown in Table 1.4, a real case.

1.9 Readout Electronics

As will be discussed throughout the next chapters of this book, not only are the silicon sensors evolving, but the involvement and evolution of the front-end electronics is probably even more impressive. Initially in the 1980s the silicon crystals were held by a frame and signals from each strip were fanned out to amplifiers held by bulky printed circuit boards (see Sect. 2.2). In a collider experiment, where space constraints in the vertex regions are very tight, a similar assembly is certainly not applicable. Fortunately, in the 1980s another development in industry and also in the universities, the *integrated circuit revolution*, made custom Application Specific Integrated Circuits (ASICs) broadly available. This initiated the opportunity for amplifier miniaturization and optimization. Without ASIC development, silicon micro vertex detectors as we know them today would not have been possible. Small electronic chips around $5 \times 5 \text{ mm}^2$ were developed serving mostly 128 sensor channels. They were placed together with some passive components on small platforms of ceramic, beryllium or flex. These platforms, called hybrids, were then attached on the end of daisy-chained sensors or sometimes even on top of the sensors itself. Photos of such assemblies can be seen in Fig. 3.7 (DELPHI hybrid), Fig. 3.6 (DELPHI module), Fig. 3.9 (DELPHI Ministrip module and pixel module) and in Fig. 5.22 (CMS components of a module).

²⁹ LHCb is one of the four detectors at the LHC, the sensors are shaped roughly as a half-moon and the round cutting was achieved by laser cutting.

Table 1.4 The different processing steps of a real double-sided sensor are listed as an example

Step	Processing Description	Days	Notes
1	Silicon selection and scribing		
2	Field oxide		Thermal at 1000°C; 0.9 µm dry + wet + dry, Ar/N
3	Image main implants	9	$p+$ on junction side, $n+$ on ohmic side. Deposit resist, open windows, etch in BOE ^a 10 min (should reach silicon), strip resist
4	Reoxidation (cap oxide)	5	Thermal at 900°C; 0.2 µm wet + dry
5	Main implants		$p+$ junction side: boron 80 keV 2E15; $n+$ ohmic side: phosphorus 150 keV 5E15
6	Image secondary implants	8	$p+$ stop on ohmic side (isolation), image n implant on junction side Etch in BOE 10 min (should reach silicon), back B+; front P+ at same time
7	Secondary implants	2	$p+$ implant on junction side: boron 20 keV 5E14 $n+$ implant on junction side: phosphorus 40 keV 5E14
8	Oxide partial strip	8	Remove 0.1 µm of SiO ₂ in BOE sulphuric and rinse, then thin down
9	Reoxidation		Thermal at 900°C; 0.1 µm wet + dry Total time at 900°C; 1 h, in steam for 20 min Three steps: Ar, O ₂ , H ₂ O
10	Poly deposition		0.7 µm 2 h at 600°C
11	Poly blanket implant	2	B+ 1.3E14, 80 keV, both sides Boron resistivity about 30 $\frac{\Omega}{\text{cm}^2}$.
12	Silox deposition	8	0.8 µm
13	Image silox for poly contacts		High-dose implant, both sides or one at a time
14	Poly high-dose implant	4	Boron resistivity about 20–100 $\frac{\Omega}{\text{cm}^2}$ on both sides
15	Image of poly, plasma etch	2	Plasma etching 10 min
16	Anneal	3	30 min at 900°C; $\sim 3000 \text{ \AA}$
17	PECVD ^b	6	0.1 µm adjusted to have 0.3 µm over implant
18	Contact (via) opening		Wet etching BOE about 2.5 min
19	Wafer cleaning		Remove about 0.01 µm of oxide
20	Metal deposition	4	Sputtered Al–Si
21	Metal imaging, wet etching	4	
22	Passivation silox deposition	3	350°C thickness 1 µm
23	Passivation window opening		Wet etch that stops on metal
24	Cutting	5	Cut and wash with de-ionized water
25	Probing		

^a BOE stands for buffered oxide etch. It is hydrofluoric acid (HF) with ammonium fluoride (NH₄F) and water to “buffer” the etching effect. Regular HF would etch too fast. The HF solution etches only SiO₂, not silicon.

^b PECVD: Plasma Enhanced Chemical Vapour Deposition.

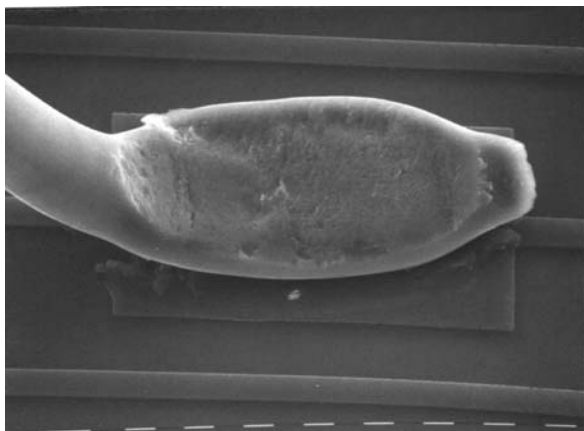


Fig. 1.49 An electron microscope picture of a bond foot. These connections are achieved via a thin wire (17 or 25 μm is standard width) bonded via ultrasonic

Chip Features

Low noise and large gain were one of the most critical requirements for the readout electronics. Signal sizes only rise to around 3.6 fC for a minimum ionizing particle in 300 μm thick silicon. Most chips work in the Double Correlated Sampling mode (DCS).³⁰ Small readout pitches of 25–100 μm require high connection density on sensor and chip side. The connection to the silicon sensors was achieved by ultrasonic wire-bonding. An electron microscope picture of a wire-bond foot attached to a silicon sensor pad is presented in Fig. 1.49. Connection pictures in the DELPHI case are presented in Fig. 3.14 on page 118, while CMS bonding is shown in Fig. 5.24 on page 170.

In addition the high number of readout channels with the given accessibility of the chips requires multiplexing and often the chip readout is only active, when a signal is present (*pulsed power mode*) to dissipate as least power as possible in the detector volume. In many cases channel signals are only read out when charges are above a certain threshold to avoid filling bandwidth with zero information (*sparsification*). In the hadron colliders, especially the LHC and the future SLHC, radiation hardness of the readout chips was one of the most difficult challenges in the last millennium. Most chips are processing pure analog signals, but some are already implementing the digitization in the front-end chip. Table 1.5 summarizes the different choices and time evolutions.

³⁰ Double correlated sampling: Charge is integrated on a capacitor C_1 with signal absent, while the charge is stored in capacitor C_2 with signal present. The charge difference between both capacitors represents the SIGNAL. This technique reduces leakage current effects.

Table 1.5 VLSI chips along the years

	Chip	Year	Feature size (μm)	Channels	Rad tolerant	Pulsed power mode	Bunch crossing	ADC	Sparsification	Pipeline depth
DELPHI	MX1	1989-90	5	128	~10 krad	yes	22 μs	analog	no	0
	MX3	1990-93	3	128	~10 krad	yes	22 μs	analog	no	0
	MX6	1994-2000	3	128	~10 krad	yes	22 μs	analog	no	0
	Triplex	1996-2000	1.2	128	~10 krad	yes	22 μs	analog	no	0
CDF	SVXD	1986-89	3	128	~12-20 krad	no	3 μs	analog	no	0
CDF	SVXH	1993-96	1.2	128	1 Mrad	no	132/396 ns	8bit	no	32
CDF	SVX3	1995-98	0.8	128	10 Mrad	no	132/396 ns	8bit	yes	42
—	SVX4	2000-03	0.25	128	50 Mrad	no	—	8bit	yes	42
CMS	APV25	2000	0.25	128	20 Mrad	no	25 ns	analog	yes	192
SLHC	***	20**	?0.065?	?1024?	yes	no	?	8-10bit	yes	many
ILC	UMC	?	0.13	128-512	yes	yes		10bit	yes	8-16

This table cannot be exhaustive, it holds chip versions of the detectors discussed in this monography. There are a multitude of other chips, e.g. the Viking or VA [128] is used on multiple occasions, the CAMEX64A used in ALEPH, the HELIX for LHCb, the ABCD for ATLAS and all of this does not even take into account the multiple pixel chips like the SP8 for DELPHI and the ROC for the CMS experiment. The field and developments are extensive with many special necessary solutions but also with many common aspects. The main “environmental” parameters are shaping time and load capacitance and the use of analog or digital circuitry complemented by the feature needs like sparsification, dead-timeless readout, etc

ASICs History

The next lines illustrate the historical evolution, improving noise values, adding features, increased readout speed, decreased feature size, always fighting against higher capacitance and high-radiation environment.

DELPHI – LEP

The first Very Large Scale Integration (VLSI)³¹ chip, the Microplex designed in Rutherford Appleton Laboratories and fabricated in Stanford University [158] was used for the MARK II [110] experiment at SLAC. It was a NMOS chip, the predecessor of all MX [14, 96] and Triplex chips used in the DELPHI (MX3, MX6 and TRIPLEX) and Opal (MX5) experiments at LEP produced in CMOS technology. These chips contained 128 channel charge-sensitive amplifiers, low noise, high gain chips for medium capacitor values with multiplex feature and pulsed power mode. In the last DELPHI upgrade stage, the TRIPLEX chip was introduced, being optimized for higher load capacitances, deriving from longer modules.

CDF – TEVATRON

The early MX chip version was also evaluated to be used in the CDF experiment at Fermilab but longer silicon modules, with higher load capacitor values initiated a new development in Berkeley, the SVX [74] chip series, which was used from 1992 to 2008 and beyond. The SVX was also the first chip designed for a high-rate environment. All SVX versions have the sparsification feature and use double correlated sampling.³² For the later CDF and D0 operating since 2000, a new dead-timeless readout chip with analog-to-digital 7-bit conversion on chip level, the SVX2/SVX3 [170] with a 46 capacitor deep storage pipeline plus one reference cell, was introduced. A total of 42 cells were used for storage, 4 as actual flagged readout buffer plus 1, which is finally utilized in the digitization process. The chip is purely digital and can be programmed. It can operate in the following modes: readout “hit channel” or the “hit channel plus neighbours” or “all channels”. The SVX3 is optimized for 396 ns and 132 ns beam crossing intervals. It is composed of a front-end (analog) part separated from the back-end (digital) part.³³ The current SVX chip version, the SVX4³⁴ [69], is produced in 0.25 μm radiation-tolerant technology and with about 30% less noise than SVX3. The SVX4 has the feature to physically decouple individual channels via a program mask, this feature is especially profitable when a channel is noisy or connected to a pinhole.

³¹ Very Large Scale Integration (VLSI) stands for the process of creating *Integrated Circuits* (ICs) by combining thousands of transistor-based circuits into a single chip.

³² In the first version, with DC coupling, even quadruple correlated sampling was used to suppress the direct current flowing into the amplifier.

³³ Initially, these parts were even produced separately, only later was a monolithic chip produced.

³⁴ It was designed for the planned RUNIIB of the TEVATRON, which was finally abandoned.

CMS – LHC

For the LHC, with much shorter bunch crossing intervals, a low-noise analog chip, the Analog Pipeline Voltage chip APV25 [66, 76, 95] was developed. The APV25 was fabricated in 0.25 μm CMOS technology³⁵ which is intrinsically radiation tolerant, when obeying some special design rules. This feature will be further discussed in Sect. 5.1.1 on page 158. The chip is optimized for the 25 ns bunch crossing at LHC. As the name says, the chip produces analog output, converted via analog-opto-hybrids to laser signals and routed via $\sim 100\text{m}$ cables to the CMS ADC,³⁶ modules located in the adjacent service cavern. With about 25000 electron-hole pairs per MIP in 300 μm thick silicon around 110 mV/MIP is expected at a sampling frequency of 40.08 MHz. The chip stores charges in a 192 elements deep pipeline to cope with the 4.8 μs trigger latency. The pipeline serves also as a means to reduce noise, avoiding very small *real* integration and shaping times. The pipeline cells are connected to the Analog Pulse Shape Processor (APSP), which works in *Peak*, *Deconvolution* or *Multimode*. Despite bunch crossings every 25 ns, the APV peaking times t_p are 50 ns long, optimized for low-noise performance. The APSP discriminates signals from consecutive bunches. Overlapping signals are *deconvoluted* by adding three consecutive peak mode samples with according weights [76], this deconvolution reduces the pulse width to 25 ns. In peak mode, each signal is read out without weighting and multimode corresponds to three consecutive peak mode signals. The signals of the 128 channels are multiplexed. A new important feature is the common mode noise suppression.³⁷

Current Designs and Future Developments

The SiTr-130 chip, one of the chip designs foreseen to be used in the *International Linear Collider* (ILC), is at the moment in the prototype stage. It is designed in 130 nm CMOS technology and incorporates the following features: preamplifier, shaper, trigger capability on analog sums, analog pipeline, analog event buffering (8–16 events) on chip 10-bit digitization, pulsed power mode and intrinsic calibration. It has buffering and preprocessing capability of centroids, least square fits, loss compression and error codes built in [59]. With the smaller feature size, thus the possibility to place a larger number of transistors per area, it is possible to implement many more features directly on the chip level. Noise values of the different chip generations are presented in Table 1.3 on page 29 where the noise-load capacitance correlation is discussed.

The initial chips were produced in a 5 μm CMOS process, followed by 3, 1.2, 0.8, 0.5, 0.25 μm in the current collider experiments. Today, there are prototype chip runs in 130 nm CMOS processes, but already discussions about 65 nm have begun for the future LHC upgrades [118]. As an interesting fact, it can be noted that already in the time of the SVX, the so-called “multiproject wafer” system was

³⁵ Quarter Micron Technology.

³⁶ Analog to Digital Converter (ADC).

³⁷ Common mode: Baseline fluctuations common for all channels of a chip.

used. To reduce cost only design files are sent to companies, which then combine projects from different groups and subcontracts a number of different vendors for mask and final chip fabrication. This is a common practice today to enable the HEP community to have several design runs for a chip at reasonable costs.

Today, quarter micron technology is radiation tolerant, when utilizing special design rules. In the future, feature sizes of 130 nm and below will be intrinsically radiation tolerant and will not even need special designs.

1.10 Radiation Damage in Silicon Detector Devices

The intent of this chapter is to introduce the radiation effects and give a general understanding of radiation damage – its mechanism, microscopic and macroscopic effects. The very basics of radiation damage are presented in [126] and [165, 166], recent studies on fully segmented sensors on a large sample can be found in [55] and [56]. The three main effects (bulk and surface defects) introduced by radiation are

- displacement of atoms from their positions in the lattice (bulk)
- transient and long-term ionization in insulator layers (surface)
- formation of interface defects (surface)

1.10.1 Bulk Damage

Detectors at the LHC and also already at the TEVATRON operate at high particle fluxes, necessary to achieve a large statistical sample on particle collisions, to understand physics of the events in a hadron collider environment. To understand the voltage or current of an irradiated sensor the following mechanisms have to be taken into account:

1. the damage to the lattice created by traversing particles
2. the following diffusion processes – annealing

The following sections describe the microscopic and macroscopic changes in the material with radiation and subsequent changes with time. The introduced models describe the evolution of sensor parameters like leakage current, depletion voltage and Charge Collection Efficiency (CCE). A significant dependency on the type of radiation particle exists. In addition, for charged particles, a strong dependence is seen for different radiated silicon materials – especially on their oxygen or carbon content. The models, with the initial constants, describe the data very well. But for a large production, it is strongly advised to launch a dedicated radiation campaign allowing subsequently the re-fit of Hamburg model parameters for the specific sensors.

Damage by Particles

Traversing particles are not only ionizing the lattice but they also interact with the atomic bodies via the electromagnetic and strong forces. Atoms are displaced and

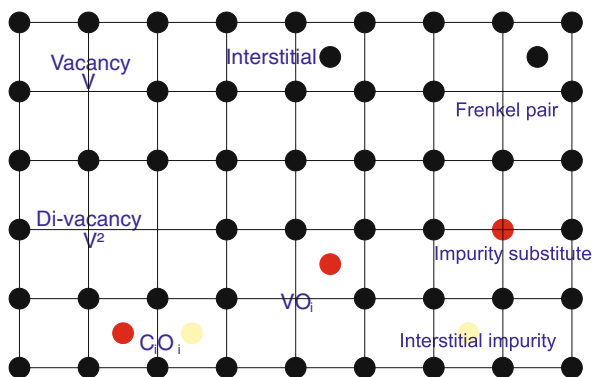


Fig. 1.50 The figure shows an exemplary selection of atomic displacements in the lattice after collision with traversing particles. These vacancies, interstitials and complex clusters are creating new levels in the energy scheme of the semiconductor and therefore change the elementary properties. As abbreviation, vacancies are labeled V , interstitials I , di-vacancies V_2 . Impurities are labeled with their atomic sign, their index defines their position as substitute or interstitial, e.g. C_s or C_i

create interstitials I , vacancies V and more complex constructs, e.g. di-vacancies V_2 or even triple-vacancies V_3 , also di-interstitials I_2 are common. All these defects deform the lattice. Some examples are depicted in Fig. 1.50. In addition diffusing Si atoms or vacancies often form combinations with impurity atoms, like oxygen, phosphorus or carbon, again with different properties. All these lattice displacements populate new levels with no beneficial or malevolent results for detector operation in the band gap, changing the initial silicon properties. The resulting macroscopic property changes are

- increase of dark current
- change of depletion voltage level (N_{eff}) due to creation of mainly additional acceptor levels
- decrease of charge collection efficiency due to defect creation, acting as traps

The basic important levels and their roles and macroscopic effects are shown in Fig. 1.51. Defect analysis and even defect engineering was started in the R&D collaboration Rose/RD48³⁸ and is nowadays continued with the RD50 collaboration at CERN. Within this chapter the basic mechanisms are described, special cases and defect engineering will be described in Chap. 5 and Sect. 6.1. The topic of defect engineering is fully covered and up to date in [147]. For example vacancy plus phosphorus VP removes the donor property of single phosphorus. A special case is the di-vacancy plus oxygen combination V_2O , which introduces additional negative space charge. A detailed table of defect combinations and respective quantitative energy levels can be found in [111, 126]. The defect distribution and clustering in Fig. 1.52 clearly show the difference between charged and neutral particles and their different energy levels. Especially the additional Coulomb force of a charged particle enhances small energy transfer and therefore local short distance defects, known as Frenkel pairs. Neutral particles, like neutrons, acting via

³⁸ ROSE: R&D On Silicon for future Experiments.

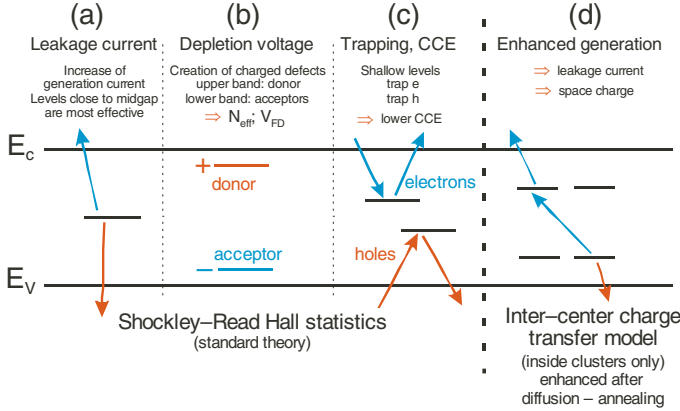


Fig. 1.51 The different defect level locations and their effects. All relevant defect levels due to radiation are located in the forbidden energy gap. **(a)** Mid-gap levels are mainly responsible for dark current generation, according to the Shockley–Read–Hall statistics and decreasing the charge carrier lifetime of the material. **(b)** Donors in the upper half of the band gap and acceptors in the lower half can contribute to the effective space charge. **(c)** Deep levels, with trapping times larger than the detector electronics peaking time, are detrimental. Charge is “lost”, the signal decreases and the charge collection efficiency is degraded. Defects can trap electrons or holes. **(d)** The theory of inter-centre charge transfer model says that combinations of the different defects in so-called defect clusters additionally enhance the effects

the strong force result mainly in long-range cluster defects. With enough energy the initial PKA³⁹ acts further on several additional lattice atoms. In the non-relativistic approach, the maximum transferred energy $E_{R,max}$ can be calculated in the case of recoil for a particle with mass m_p and kinetic energy E_p with

$$E_{R,max} = 4E_p \frac{m_p m_{Si}}{(m_p + m_{Si})^2} \quad (1.45)$$

For electrons with energy E_e and mass m_e , higher kinetic energies are needed for lattice damage. $E_{R,max}$ can be calculated by the approximate relativistic relation

$$E_{R,max} = 2E_e \frac{E_e + 2m_e c^2}{m_{Si} c^2} \quad (1.46)$$

Table 1.6 shows the average and maximum energy transfer of different particle types with the incident energy of 1 MeV.

Also, the energies needed to knock an atom from its original lattice place are clearly dependent on the binding forces and therefore on the material. In the case of silicon, the minimum energy needed to displace a single lattice atom (Frenkel pair) is $E_{single\ defect} \approx 25\text{ eV}$, while $E_{cluster} \approx 5\text{ keV}$ is needed to produce a defect cluster. Table 1.7 lists the minimum kinetic particle energies needed to transfer $E_{single\ defect}$ or $E_{cluster}$, subsequently creating a single point defect or a cluster.

³⁹ PKA: Primary Knock on Atom.

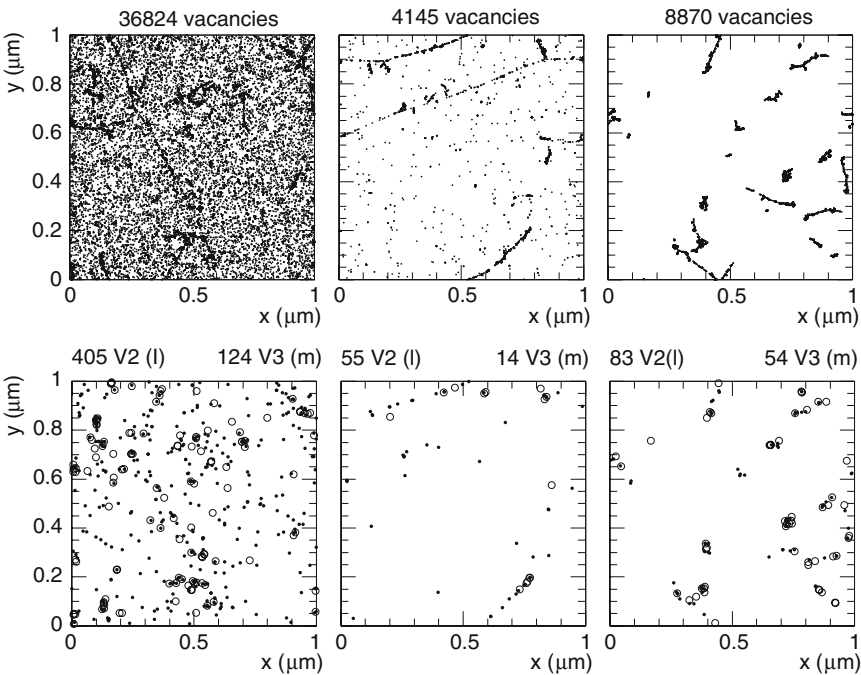


Fig. 1.52 Simulation of defect formation with radiation and diffusion. The upper three simulations show the microscopic picture of defect distribution. About 10 MeV protons (*left*) produce a quite homogeneous vacancy distribution, while more energetic protons with 24 GeV (*middle*) form more clustered and discrete defects. Neutrons with 1 MeV (*right*), interacting only due to strong interaction, do produce more isolated clustered defects. The plots are projections over 1 μm of depth (z) and correspond to a fluence of $10^{14} n_{\text{IMeV}}/\text{cm}^2$. The *lower three* figures are displaying final constellations after a certain annealing time and therefore diffusion effects occurred. Many initial defects decay, e.g. Frenkel pairs, where interstitials recombine with vacancies. Others form more local clusters, like formations of di- and triple vacancies, with again different levels and therefore different properties. The full study is described in [91]

Table 1.6 Maximum energy transfer ($E_{\text{Recoil,max}}$) vs. average ($E_{\text{Recoil,av}}$) of different particle types with incident energy of 1 MeV. Clearly the long-ranging Coulomb force favours a small energy transfer and therefore point defects, while the strong force produces mostly clusters

	Electron	Proton	Neutron	Si ⁺
Force	Coulomb	Coulomb and nuclear	Elastic nuclear	Coulomb
$E_{R,max}[\text{keV}]/E_{R,av}[\text{keV}]$	0.155/0.046	133.7/0.21	133.9/50	1000/0.265

The NIEL⁴⁰ hypothesis allows a first-order normalization of radiation damage with respect to different particles with different energies, see also Table 1.7. The displacement damage $D(E)$ can be calculated by

⁴⁰ NIEL: Non Ionizing Energy Loss.

Table 1.7 The minimum kinetic particle energies to create single point or cluster defects can be derived with formula 1.45 (p and n) and 1.46 (e^-). The ^{60}Co -photons could only create a cluster defect via a secondary electron (dominantly via Compton effect), but it cannot energize e^- up to 8 MeV

Particle	$E_{\text{single defect}}$	E_{cluster}
neutron; protons	185 eV	35 keV
electrons	225 keV	8 MeV
^{60}Co -gammas	1 MeV	No cluster

$$D(E) = \sum_i \sigma_i(E_{\text{kin}}) \int_0^{E_{R,\text{max}}} f_i(E_{\text{kin}}, E_R) P(E_R) dE_R \quad (1.47)$$

where all possible interactions are summed up. σ_i is the cross section of the process and $f_i(E, T)$ is the probability of having a collision of a particle with E_{kin} , transferring a recoil energy of E_R . $P(E_R)$ is the Lindhard partition function [109], describing the fraction of energy going into silicon atom displacement, e.g. $P(E_R) \approx 50\%$ for 10 MeV protons or $P(E_R) \approx 42\%$ for 24 GeV protons and $P(E_R) \approx 43\%$ for 1 MeV neutrons [91]. The resulting displacement functions are plotted in Fig. 1.53. As standard the 1 MeV *neutron equivalent fluence* [$n_{1\text{MeV}}/\text{cm}^2$] is used and abbreviated with Φ_{eq} , corresponding to $D_{\text{neutron}}(1\text{ MeV})/\text{cm}^2 = 95\text{ MeV mb}/\text{cm}^2$, with Millibarn: $\text{mb} = 10^{-27}\text{ cm}^2$. It is therefore possible to scale radiation damage from different particles and different energies by a simple numerical factor κ to make comparison possible. κ is defined as the ratio of the individual damage particle factor for a given energy and 1 MeV neutrons.

$$\kappa = \frac{\int D(E) \phi(E) dE}{95\text{ MeV mb} \cdot \Phi} = \frac{\Phi_{eq}}{\Phi} \quad (1.48)$$

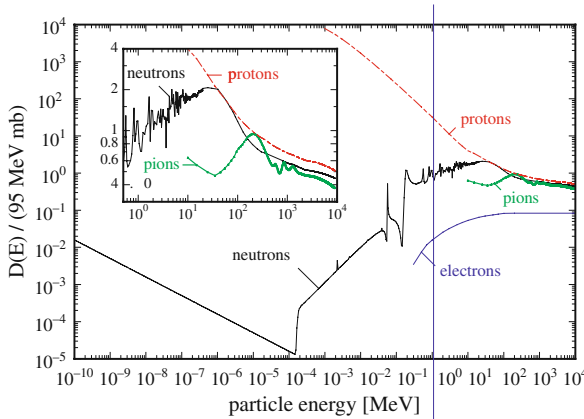


Fig. 1.53 NIEL – non ionizing energy loss. Displacement damage function $D(E)$ normalized to 95 MeVmb for neutrons, protons, pions and electrons. The inserted graph shows a detail of the figure around relevant energies for high-energy physics [91, 126]

where $\phi = \int \phi(E)dE$ is the irradiation fluence. The 1 MeV neutron equivalent fluence Φ_{eq} is then calculated by

$$\Phi_{eq} = \kappa \Phi = \kappa \int \phi(E)dE; \quad [\Phi_{eq}] = n_{1\text{MeV}}/\text{cm}^2 \quad (1.49)$$

In plots and in literature the $n_{1\text{MeV}}/\text{cm}^2$ unit is often omitted and without specific reference to a particle type all fluences are given as 1 MeV neutron equivalent.

Leakage Currents

Mid-gap defects are constantly produced during radiation. They degrade mainly the lifetime τ , being efficient electron–hole pair generators they therefore increase the dark currents. It was found in many experiments that there is a linear behaviour of dark current vs. fluence.

$$\frac{\Delta I}{V} = \alpha \Phi_{eq} \quad (1.50)$$

where V normalizes for a given volume. α is called the current-related damage rate. The correspondence is shown in the left part of Fig. 1.54. The good linearity over several orders of magnitude allows the technical use of diodes to determine the particle fluence by the increase of current.

Depletion Voltage

The situation for the effective space charge concentration is a bit more difficult. It is displayed in Fig. 1.55. Starting with an n -type-doped silicon bulk, a constant removal of donors ($P + V \rightarrow VP$ centre) together with an increase of acceptor-like levels (one example is $V + V + O \rightarrow V_2O$) shifts the space charge first down to an intrinsic level and then up to a more p -like substance. The material “type inverts”. The depletion voltage therefore drops first and starts rising later. Figure 5.17 in Sect. 5.1.2 shows an example of the CMS sensor irradiation campaign and the evolution of depletion voltage. With

$$N_{eff} = N_{D,0}e^{-c_D\Phi_{eq}} - N_{A,0}e^{-c_A\Phi_{eq}} - b\Phi_{eq} \quad (1.51)$$

the evolution of N_{eff} can be parameterized in first approximation with the donor and acceptor removal rates c_D and c_A plus the most important acceptor creation term $b\Phi_{eq}$. Since there is a significant temperature-dependent diffusion,⁴¹ Formula (1.57) parameterizes the evolution in a more common and general description.

⁴¹ The term “diffusion” used here is more a descriptive one combining effects like diffusion, migration, break-up, re-configuration of defects – also often summarized by the term “annealing”.

Charge Trapping

The trapping rate is proportional to the concentration of trapping centres N_i , resulting from defects. Therefore the trapping probability can be formulated by

$$\frac{1}{\tau_{eff}} = \sum_i N_i (1 - P_i) \sigma_i v_{th} \quad (1.52)$$

with P_i the occupation probability and σ_i the charge carrier cross section. In first order the fluence dependence is linear and can be written as

$$N_i = g_i \Phi_{eq} f_i(t) \Rightarrow \frac{1}{\tau_{eff}} = \gamma \Phi_{eq} \quad (1.53)$$

with the introduction rate g_i ; $f_i(t)$ describes the annealing with time. An example is plotted in Fig. 1.58 (left side). The slope is different for electron and hole trapping, they are differently affected due to their different mobilities. Some initial numbers for proton and neutron irradiations are given in Table 1.8.

The degradation of Charge Collection Efficiency (CCE) can then be described by

$$Q_{e,h}(t) = Q_{0,e,h} \exp\left(-\frac{1}{\tau_{eff,e,h}} \cdot t\right), \text{ where } \frac{1}{\tau_{eff,e,h}} \propto N_{defects} \quad (1.54)$$

At effective fluences of $\Phi_{eq} = 10^{15} \text{ n}_1 \text{ MeV/cm}^2$ and above, trapping becomes the most limiting factor of silicon usage as a particle detector. The charges no longer arrive at the collecting electrodes in 300 μm thick sensors. Examples of charge travelling distances x for $\Phi_{eq} = 10^{15} \text{ n}_1 \text{ MeV/cm}^2$ and $\Phi_{eq} = 10^{16} \text{ n}_1 \text{ MeV/cm}^2$ are

- $\tau_{eff}(10^{15} \text{ n}_1 \text{ MeV/cm}^2) = 2 \text{ ns}$: $x = v_{sat} \cdot \tau_{eff} = (10^7 \text{ cm/s}) \cdot 2 \cdot \text{ns} = 200 \mu\text{m}$
- $\tau_{eff}(10^{16} \text{ n}_1 \text{ MeV/cm}^2) = 0.2 \text{ ns}$: $x = (10^7 \text{ cm/s}) \cdot 0.2 \cdot \text{ns} = 20 \mu\text{m}$

The following list summarizes the main operation limiting effects of radiation bulk damages for the different Φ_{eq} levels:

- at $10^{14} \text{ n}_1 \text{ MeV/cm}^2$ the main problem is the increase of leakage current
- at $10^{15} \text{ n}_1 \text{ MeV/cm}^2$ the high resulting depletion voltage is problematic
- at $10^{16} \text{ n}_1 \text{ MeV/cm}^2$ the fundamental problem is the CCE degradation

Table 1.8 Introduction of trapping centres, significant for electrons and holes of neutron and proton radiations [106]

	$\gamma_{e,0} [10^{-16} \text{ cm}^2/\text{ns}] \text{ for Electron}$	$\gamma_{h,0} [10^{-16} \text{ cm}^2/\text{ns}] \text{ for Holes}$
Proton	(4.97 ± 0.14)	(5.25 ± 0.17)
Neutron	(3.53 ± 0.24)	(5.10 ± 0.39)

Annealing – Diffusion of Defects

Interstitials and vacancies are very mobile at temperatures $T > 150$ K. The lower part of Fig. 1.52 displays the result of defect diffusion. Basically, there is the possibility of

- Frenkel pair recombination ($I + Si_V \rightarrow Si$)
- vacancy and interstitial combination (e.g. $V + V \rightarrow V_2$)
- combination of more complex defects (e.g. $C_i + O_i \rightarrow C_iO_i$)

where the former types are short-range and very mobile processes and therefore happen with a shorter time constant, while the latter happens with a longer time constant. The whole process is called *annealing* with a beneficial part reducing the damage and a reverse annealing part degrading macroscopic sensor properties. Some parts are stable and do not evolve with time. The diffusion processes are naturally temperature dependent and some effects, e.g. depletion voltage evolution, can even be frozen out at temperatures below 0°C. In addition, different levels in the energy band behave differently with respect to time constants and temperatures.

Annealing — Leakage Current

The annealing of the dark currents is displayed in the right part of Fig. 1.54.

The α parameter, respectively the dark currents, can be parameterized. In first order α can be fitted by a sum of exponentials, pointing to the existence of several contributing defects with different decay time constants. The radiation afflicted current continuously decays exponentially until it follows more or less a logarithmic behaviour or even saturates for higher temperatures after several months. According to [126] the annealing behaviour can be described by

$$\alpha = \alpha_0 + \alpha_I e^{-\frac{t}{\tau_I}} - \beta \cdot \ln \frac{t}{t_0} \quad (1.55)$$

with $\alpha_I \sim 1.25 \cdot 10^{-17}$ A/cm, $\beta \sim 3 \cdot 10^{-18}$ A/cm and $t_0 = 1$ min. τ_I takes the annealing temperature T_α dependence into account, where

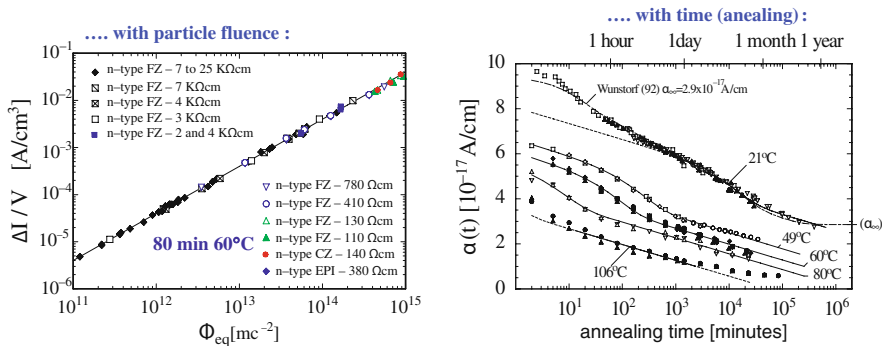


Fig. 1.54 Leakage current vs. fluence and annealing time [126, 166]

Table 1.9 α and τ_I for different temperatures

Annealing temperature in °C	21	40	60	80
α_0 in 10^{-17} A/cm	7	6	5	4
τ_I in min	140000	260	94	9

The table shows the α parameter and the time constants τ_I for the current annealing for different temperatures. Below room temperature the time constants are longer than 100 days and annealing is almost frozen out.

$$\frac{1}{\tau_I} = k_{0I} \cdot e^{-\frac{E_{gap}}{k_B T \alpha}} \quad (1.56)$$

with $k_{0I} = 1.2^{+5.3}_{-1.0} \cdot 10^{13} \text{ s}^{-1}$, e.g. $\tau_I \approx 10$ days at room temperature. $\alpha_0 = -(8.9 \pm 1.3) \cdot 10^{-17} \text{ A/cm} + (4.6 \pm 0.4) \cdot 10^{-14} \text{ AK/cm} \cdot \frac{1}{T\alpha}$ is a fitted parameter dependent on the annealing temperature. Table 1.9 gives α and T_I examples for different temperatures.

The average α after a standard annealing scenario of 80 min at 60°C is $4 \cdot 10^{-17} \text{ A/cm}$, measured at room temperature. The effect is temperature dependent and also effective but strongly reduced at sub-zero temperatures. Different from the time dependence of the depletion voltage, which starts to rise at later times, the current annealing always decreases the dark current and is therefore only “beneficial”.

Annealing — Depletion Voltage

The annealing of N_{eff} and therefore the depletion voltage evolution can be described by

$$\Delta N_{eff}(\Phi_{eq}, t, T) = N_{C,0}(\Phi_{eq}) + N_A(\Phi_{eq}, t, T) + N_Y(\Phi_{eq}, t, T) \quad (1.57)$$

where Φ_{eq} stands for 1 MeV neutron equivalent fluence, with the stable term $N_{C,0}$, the short-term annealing term N_A and the second-order long term N_Y . This description is called the Hamburg model and it is depicted in the right part of Fig. 1.55. In its basic nature it parameterizes the space charge change due to donor removal plus acceptor creation with fluence and latter annealing. It was proposed in [126] and with some adaptation of the initial time constants to the different sensors it has been very successful.

Before discussing the three annealing terms in some detail, it must be mentioned that the stable term is the most relevant one in a high-radiation environment. For the LHC experiments, the beneficial annealing needs to be exploited during the maintenance periods to heal the short-range defects and therefore reduce the depletion voltage, while the reverse annealing term needs to be suppressed by freezing out at sub-zero temperatures, both are possible. It also has to be mentioned that all constants in this chapter are taken from [126] and need to be re-fitted for the user case, see e.g. [161], some constants reflect, for example, the oxygen content. As an example, Fig. 1.56 illustrates the CMS radiation campaign, where sensors were subjected to several fluences and annealing parameters were fitted.

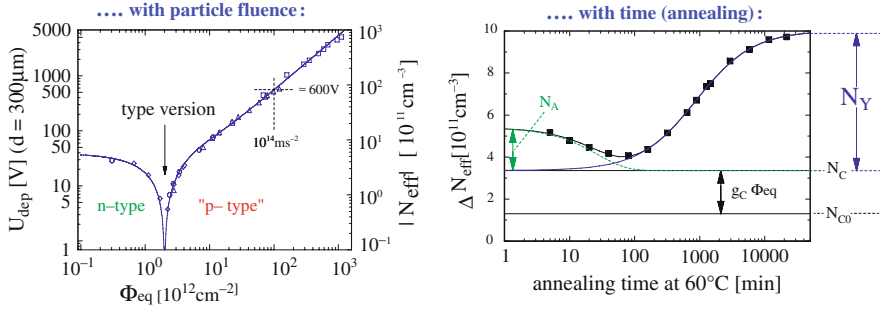


Fig. 1.55 Depletion voltage current vs. fluence and annealing time [126]

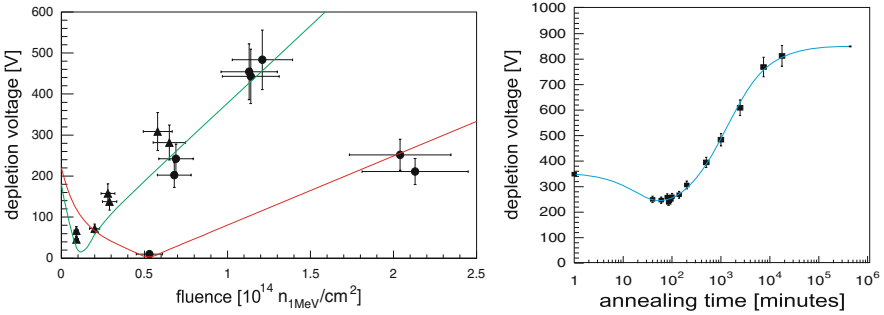


Fig. 1.56 Evolution of V_{FD} for different fluences and annealing durations. To have a basis for radiation evaluation, CMS irradiated several sensors and modules to get actual adapted fit parameters to the Hamburg model for the specific procured sensors. In this case, the beneficial constants g_a were found to be $1.11 \pm 0.16 \cdot 10^{-2} \text{ cm}^{-1}$ and $t_a(60^\circ\text{C}) = 21 \pm 8 \text{ min}$; the reverse constants are $G_y = 4.91 \pm 0.27 \cdot 10^{-2} \text{ cm}^{-1}$ and $t_y(60^\circ\text{C}) = 1290 \pm 262 \text{ min}$.

The different V_{FD} curve behaviours in the *left plot* can be explained by the different sensor thicknesses of $500 \mu\text{m}$ (upper curve) and $320 \mu\text{m}$ (lower curve) – mind $V_{FD} \sim N_{eff} \cdot D^2$. At fluences of 10^{14} , V_{FD} of the thick sensor would have increased above 1000 V . The initial compatible V_{FD} values are due to the different sensor resistivities. Data are compared to calculations for an annealing time of 80 min and an annealing temperature of 60°C at each fluence step. More about this study is described in Sect. 5.1.2 and [162]

The Stable Term $N_{C,0}$

In the current understanding, the stable damage term consists of two components, the donor removal and the acceptor creation rate.

$$N_C(\Phi_{eq}) = N_{C,0}(1 - e^{-c\Phi_{eq}}) + g_c\Phi_{eq} \quad (1.58)$$

where c is the donor removal constant and $N_{C,0}/N_{eff,non-irradiated}$ is the fraction of donor removal, depending strongly on the oxygen concentration, where oxygen can bind vacancies, which would otherwise combine with phosphorus ($V + O \rightarrow VO$ instead of $V + P \rightarrow VP$). This is of course grandly simplified.

Michael Moll – spokesperson of the RD50 collaboration responds to this subject:

The donor removal component of the Hamburg model can not be described by a simple process $V + P \rightarrow VP$ only. There is something more behind that and we still do not exactly understand what it is.

Ranges from 10 to 80% donor removal are observed after neutron irradiation. On average the initial donor removal rate is $N_{C,0} \cdot c = (7.5 \pm 0.6) \cdot 10^{-2} \text{ cm}^{-1}$. The second term describes a creation rate of stable acceptors with an average measured $g_c = (1.49 \pm 0.04) \cdot 10^{-2} \text{ cm}^{-1}$. Neither terms are time dependent as there are no evolutionary diffusion processes.

The Short-Term Annealing N_A , the Beneficial One

Monitoring the sensors directly after irradiation, a fast change of the depletion voltage can be observed. For type-inverted material V_{FD} decreases with time, while it increases before type inversion. This can easily be interpreted as an increase of the effective doping concentration N_{eff} . The introduced acceptors decay and inverted sensors with negative space charges become less negative while sensors that are not type inverted with positive space charge become more positive.⁴² The decay of defects can be factorized in a series of first-order exponential decays. In extremely long duration HEP experiments, the short time constants of minutes and hours are not relevant and the series can be reduced to

$$N_A(\Phi_{eq}, t) = \Phi_{eq} g_a e^{-\frac{t}{\tau_a}}; \quad N_A = g_a \Phi_{eq} \quad (1.59)$$

The average value of $g_a = (1.81 \pm 0.14) \cdot 10^{-2} \text{ cm}^{-1}$ was determined. The time constants τ_a , describing diffusion processes, are naturally temperature dependent and can be parameterized by

$$\frac{1}{\tau_a} = k_a = k_{0a} \cdot e^{-\frac{E_{aa}}{k_B T_a}} \text{ with } E_{aa} = (1.09 \pm 0.03) \text{ eV and } k_{0a} = 2.4_{-0.8}^{+1.2} \cdot 10^{13} \text{ s}^{-1} \quad (1.60)$$

They are summarized in Table 1.10 together with the time constants τ_y describing the reverse annealing term.

The Long-Term Annealing N_Y , the Reverse One

After a long time another first-order effect,⁴³ with another time constant τ_y , becomes effective – reverse annealing. Space charge becomes even more negative, more acceptor levels form. Reverse annealing can be parameterized by

⁴² Reminder: acceptors are introducing negative, donors respectively positive, space charge.

⁴³ Reverse annealing is also often described in literature (e.g. [65, 138, 139]) as a second-order effect with a parameterization of $\left[1 - \frac{1}{1+t/\tau_y}\right]$, describing accurately N_{eff} vs. time for long annealing times at higher temperatures. Nevertheless, the physical mechanism is ruled out due to the missing dependency of the effect on fluence. The rate, depending on the probability of **two** defects combining, does not increase with the number of defects.

Table 1.10 Annealing time constants; beneficial and reverse annealing. [126]

Annealing temperature [°C]	−10	0	10	20	40	60	80
Short-term annealing τ_a	306 d	53 d	10 d	55 h	4 h	19 min	2 min
Reverse annealing τ_Y	516 y	61 y	8 y	475 d	17 d	21 h	92 min

The numbers define immediately the running and maintenance conditions of experiments in a high-radiation environment. Operation temperatures below 0°C freeze out the reverse term completely and largely the beneficial one. During the maintenance periods the detectors temperatures should be elevated in a controlled way to benefit from the short-term annealing and to absolutely avoid the reverse one. An example of the foreseen maintenance scenarios of CMS are described in Sect. 5.1.2.

$$N_Y = N_{Y,0} \cdot (1 - e^{-t/\tau_Y}) \quad (1.61)$$

with

$$N_{Y,0,particle} = g_{Y,particle} \cdot \Phi_{eq} \quad (1.62)$$

being directly proportional to the particle fluence, with the introduction rate $g_{Y,particle}$ depending on the radiation type, e.g. $g_{Y,neutron} = 4.8 \cdot 10^{-2} \text{ cm}^{-1}$. Time constants are given in Table 1.10. The diffusion is temperature dependent and can be described after [126] by

$$\frac{1}{\tau_Y} = k_Y = k_{0,Y} \cdot e^{-\frac{E_{YY}}{k_b T_a}} \quad \text{with } k_{0,Y} = 7.4 \cdot 10^{14} \text{ s}^{-1} \text{ and } E_{YY} = 1.325 \text{ eV} \quad (1.63)$$

The full depletion voltage evolution with respect to fluence and time for a fixed temperature is presented in a condensed form in Fig. 1.57.

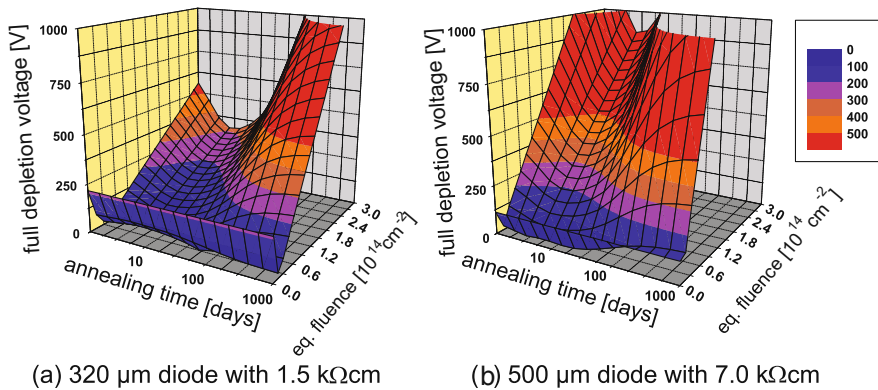


Fig. 1.57 Depletion voltage vs. fluence and annealing time. The plot shows the simulated depletion voltages according to the Hamburg model for 300 and 500 μm thick silicon, the two CMS sensor configurations. The ordinate shows the depletion voltage vs. fluence and temperature. For detector operation in high-radiation environment, it is clearly necessary to make use of the annealing up to the point where the reverse annealing becomes too strong. Of course there is one plot to be drawn per temperature, which defines the annealing time constants [56]

Annealing of Charge Collection Efficiency (CCE) – Trapping

Formula (1.53) already introduced the term $f_i(t)$ and the proportional factor γ . Experimental data show a decreasing probability of electron trapping and an increase of hole trapping in time. The right part of Fig. 1.58 shows the CCE annealing.

$$\gamma(t) = \frac{1}{\tau_{eff}} = \frac{1}{\tau_0} \cdot e^{-\frac{t}{\tau_a}} + \frac{1}{\tau_\infty} (1 - e^{-\frac{t}{\tau_a}}) \quad (1.64)$$

Still today, the statistical sample is not large, especially not on low-temperature samples. Saturation already starts after several hours at $T = 60^\circ\text{C}$, when the annealing time constants τ_a for electrons and holes are on the order of hours at elevated temperatures. The effect counts for roughly 20% for electrons and 20–50% for holes. It can be neglected at sub-zero temperatures. Pixel detectors⁴⁴ at ATLAS and CMS even benefit from the fact that inverse trapping times decrease for electrons and therefore CCE increases with time.

To summarize, the macroscopic changes deriving from diffusion, called annealing, are highly temperature dependent, while frozen out at sub-zero temperatures they are dominant at room temperature and above. Leakage current, CCE and depletion voltages evolve in the following way:

- leakage current always decreases
- charge collection efficiency decreases for holes and increases for electrons
- acceptor levels first decay in the beneficial phase and increase later in the reverse annealing phase. This leads to an increase/decrease of depletion voltage before and decrease/increase after type inversion.

The recipe is to benefit from the beneficial annealing for voltage and current and avoid the reverse annealing phase to stay in applicable bias voltage levels.

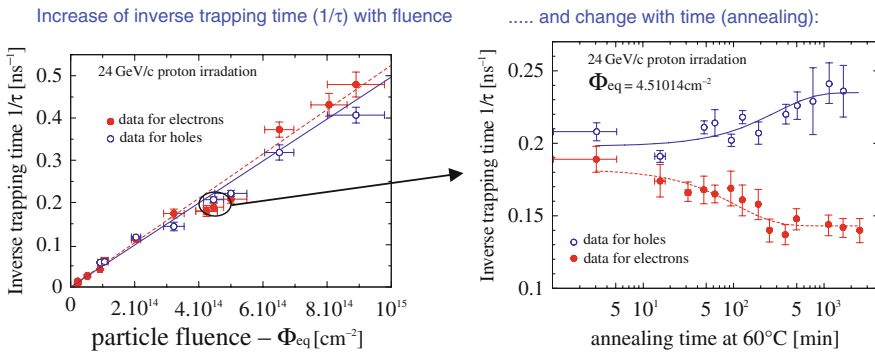


Fig. 1.58 Trapping time vs. fluence and annealing time [106]

⁴⁴ ATLAS and CMS pixels use *n*-in-*n* technology and collect electrons, while the standard strip sensors are *p*-in-*n* and collect holes.

Defect Engineering – One Example

It was mentioned, in the last sections, that impurities can influence the radiation hardness. Due to meticulous studies, mostly in the framework of RD48 and RD50, several influences are understood at the microscopic level or at least empirically on the macroscopic level. A lot of different silicon sensor substrates with several types of diffused atoms were investigated, e.g. oxygenated, carbonated, *Li*-covered, etc. Substrates created with different growth techniques were investigated and irradiated to several fluence levels, e.g. FZ, CZ, magnetic CZ,⁴⁵ epitaxial material. To present all studies is beyond the scope of this book.

Today, the most important beneficial effect identified was that for oxygen-enriched material the stable damage parameter g_c decreased and the reverse annealing time constant τ_r increased. However, this effect is only valid for irradiation by charged particles.⁴⁶ The effect can be technologically exploited. Today, the pixel sensors of the ATLAS and CMS experiment are oxygenated. The beneficial effect of high oxygen concentration and the degrading effect of carbon content are shown in Fig. 1.59.

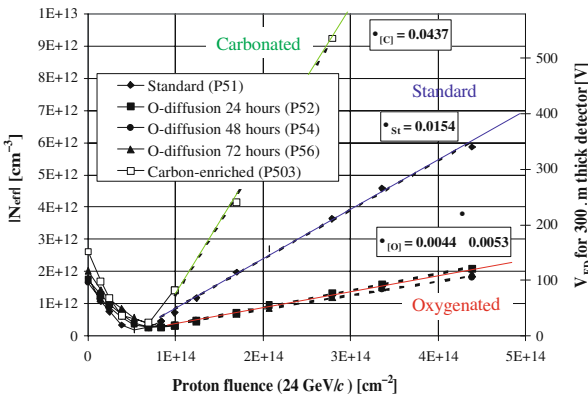


Fig. 1.59 Evolution of V_{FD} vs. time of differently engineered silicon diodes. The beneficial influence of oxygen and malevolent effect of carbon are clearly visible. Today the ATLAS and CMS pixel sensors are composed of oxygenated silicon sensors [Courtesy of RD48 and RD50]

1.10.2 Surface Damage

The term surface damage describes all radiation-induced damages in the SiO_2 layer and in the SiO_2 – Si interface. This effect is therefore prominent in AC-coupled sensors and in the NMOS and PMOS transistors of all kinds of electronics.

The damage is introduced by ionization not atomic displacement, unlike in the silicon bulk described earlier. In contrast to the situation in the silicon bulk, creation

⁴⁵ MCz: CZ crystal growth in a magnetic field to achieve a homogeneous oxygen distribution.

⁴⁶ Note that this violates the NIEL hypothesis.

of electron–hole pairs is not fully reversible in an insulator. Depending on the oxide quality, recombination varies between several percent and almost 100%. In addition to recombination, generated charge carriers can also be captured by existing defects, where the emission is highly suppressed, since the band gap is much larger in oxide and nitride layers ($E_g = 8.8 \text{ eV}$ in SiO_2 and $E_g = 5 \text{ eV}$ in Si_3N_4). In the oxide, the mobility of electrons ($\mu_{e,\text{SiO}_2} \approx 20 \frac{\text{cm}^2}{\text{Vs}}$) is several orders of magnitude higher in the oxide than that of holes ($\mu_{h,\text{SiO}_2} \approx 2 \cdot 10^{-5} \frac{\text{cm}^2}{\text{Vs}}$). This leads to a fast separation of electron–hole pairs. Electrons drift to the metal electrode, while the holes drift via a hopping mechanism via shallow levels to the Si-SiO_2 interface, especially when a voltage is applied (Fig. 1.60). The effect is enhanced for a positive voltage applied on the metal side during radiation; electron movement is accelerated to the metal side and holes drift to the interface, a standard mode for a transistor. In addition the defect concentration is especially high at the interface due to lattice mismatch and dangling bonds. The trap density in the interface region is around $10^9\text{--}10^{10} \text{ traps/cm}^2$. As a result, positive static charges accumulate at the interface, saturating at about $N_{ox} \approx 3 \cdot 10^{12} \text{ cm}^{-2}$ [167]. The introduced additional oxide volume and interface charge concentration is now increasing the flat-band voltage by

$$\Delta V_{flat} = -\frac{1}{\epsilon_{ox}\epsilon_0} \left(\sigma_{int} d_{ox} + \int_0^{d_{ox}} \varrho(x) x dx \right) \quad (1.65)$$

where d_{ox} is the oxide thickness and σ_{int} is the surface charge at the Si-SiO_2 interface and $\varrho(x)$ reflects the introduced additional charge density in the oxide volume. Therefore, measuring the flat-band voltage changes is a diagnostic tool to investigate surface damage. Negative charges are now attracted from the bulk side towards the interface and accumulate there, decreasing the inter-strip resistance and increasing polarisability, thus capacitance. For thick oxides, with a large enough positive oxide charge the depletion case can switch to electron accumulation, decreasing inter-strip resistance. As a second step also negative traps are attracted towards the interface from the bulk side. Figure 1.61 displays the field configuration for no and high oxide

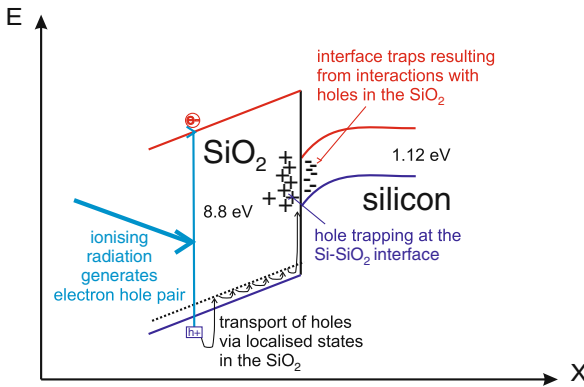


Fig. 1.60 Radiation damage in the Si-SiO_2 Interface

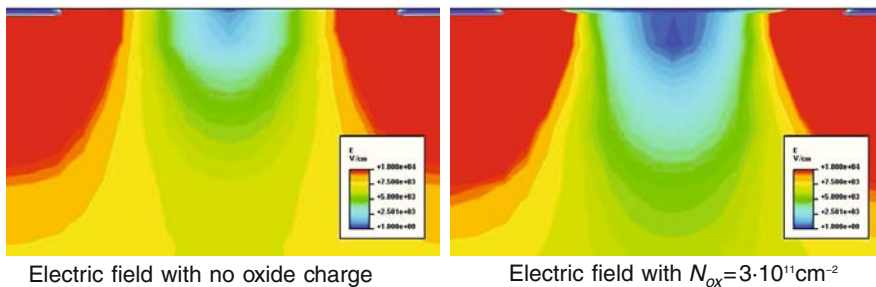


Fig. 1.61 Inter-strip region fields with/without oxide charges. The additional charges do disturb the field distribution. The low-field region in the intermediate region of the strips (right picture) allows for negative charge carriers. These are increasing polarisability and thus capacitance and are decreasing the strip-by-strip insulation, which is completely defined by the field distribution [55]

charge concentration. In Sect. 5.1.2 how the use of $\langle 100 \rangle$ silicon minimizes the effect by reducing the number of dangling bonds is described.

To summarize, due to ionization, insufficient recombination and subsequent trapping of holes at the $Si-SiO_2$ interface, the following macroscopic results deteriorate the sensor functionality.

- increase of inter-strip capacitance, thus increasing noise
- decrease of inter-strip resistance, thus increasing cross talk
- increase of flat-band voltage, as an indicator for oxide charge

A small annealing effect at high temperatures ($T \gg RT$; around 100–400°C) is also observed here, explained by the drift of bulk electrons into the near-interface region and recombination with holes trapped there. Unfortunately the reverse annealing effects at these temperatures do not allow to benefit from surface damage annealing.

While the damage mechanism in electronic circuits is the same as for the MOS structure in AC-coupled sensors, the static charge centres have several additional effects for NMOS and PMOS. Figure 1.62 shows the basic schema. The main effects are

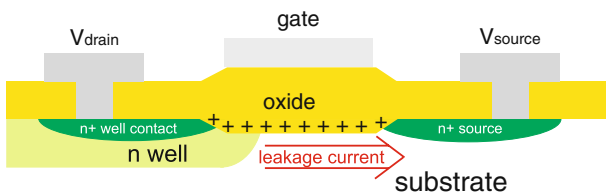


Fig. 1.62 Scheme of an NMOS transistor with deteriorating oxide charge from radiation. The oxide charge screens the gate voltage and therefore a higher threshold voltage V_{thr} is needed to operate the transistor. The resulting attracted charge carriers in the substrate region increase leakage current. The accumulating negative traps in the substrate finally affect mobility. Resulting energy levels in the mid-band region also reduce lifetime and therefore increase leakage current

- threshold voltage shift of transistor V_{thr}
- increased noise
- increased leakage current

The main drawback of radiation damage in electronics is the increase of transistor threshold voltage V_{thr} and leakage current. The increased threshold voltage derives from the screening effect of the oxide charge concentration. The shift of V_{thr} is proportional to a power n of the oxide thickness d_{ox} : $V_{thr} \propto d_{ox}^n$. The power factor n depends on the processes used to grow the oxide and its thickness. It has been measured to be in the range of 1–3. The increase of leakage current is induced by the traps acting as a mid-bandgap level introducing recombination centres, thus decreasing lifetime and therefore increasing leakage current. In addition the static traps in the interface affect the mobility in the conducting case. Finally, the accumulation of positive charges in the oxide, especially in thick oxides, can form parasitic charge transfer paths in the substrate by creating inversion layers between n -wells in the substrate. This can lead to a decrease in the signal-to-noise ratio or even to short circuits in the transistor. In the case of NMOS transistors, the charge-up of the oxide may reach a concentration that makes it impossible to completely switch off the transistor.

In Sect. 5.1.1 on page 158 the enclosed transistor design together with the deep sub-micron processing is described which is the key technology for radiation-tolerant electronics.

1.11 Other Silicon Detector Types

In this section different silicon-based detectors are shortly described. Pixel devices HAPS, CMOS and SOI sensors are introduced. Silicon drift detectors are used as an alternative 2D position sensing device. DEPFETs are developments where charge amplification is introduced in contrast to standard devices. The 3D detectors are deviations from standard planar processing mainly developed for harsh radiation environments.

1.11.1 Hybrid Pixels – An Alternative with a High Number of Channels

The full name is *Hybrid Active Pixel Sensor* (HAPS). The technological difference between silicon strip sensors and silicon hybrid pixel sensors is marginal. The strips are segmented further down to a pixel structure (e.g. strips $100 \times 150 \mu\text{m}$), the readout is adapted to small capacitances and is designed to handle DC coupling to the pixel implants. Consequently, the connection of the small structures to readout electronics is not possible with the standard wire-bonding anymore. The solution is a readout chip the size of the sensor with the same channel “pixellation” as the

sensor which is placed in a sandwich configuration on top of the sensor. It is “bump bonded” or “flip-chip-bonded” to the sensor. The pads on the sensor and readout chip are treated with a special under-bump metallization. A lithography step opens holes in the applied photoresist over the pads and a dedicated bump metal is filled in the holes. After removing the resist, the bumps are shortly heated to reflow into balls. Finally the readout chip is flipped, aligned and pressed onto the sensor. Another short heating step connects readout to sensor. There are several recipes for a sturdy bump connection, e.g. Cu as bump on a PbSn surface or an indium bump on a “UMB” (sandwich of Ti, Ni, Au). A cartoon of the bump bonding processing steps and a HAPS scheme can be found in Fig. 1.63 while a picture of actual bumps and bump bond pass can be seen in Fig. 1.64.

The obvious benefit of 2D information from pixel detector comes with the prize of a huge number of channels to be handled. The $\sim 1 \text{ m}^2$ pixel detector of CMS has about 66 million channels, about 6.6 times the channel number of the 206 m^2 strip detector. HAPS always comes with sparse readout, where only pixels with signal are read out. Due to the DC coupling a current compensation circuit to counter the dark current is needed in addition to the pixel amplifier. The granularity is limited by the minimum size of the bumps but still suits all the needs of HEP detectors.

HAPS were first used in the DELPHI experiment in the forward region, the example is described in Sect. 3.2 with a pixel module picture, refer to Fig. 3.9. In the

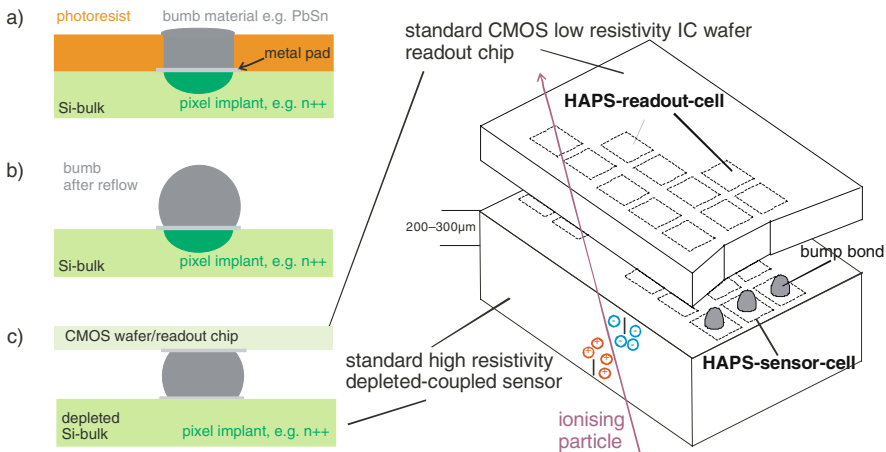


Fig. 1.63 Scheme of a *Hybrid Active Pixel Sensor* (HAPS). A HAPS is a sandwich of a silicon sensor and a standard CMOS readout chip. The sensor is of the high resistivity-depleted DC-coupled type processed as described in Sect. 1.8.2. The readout chip is realized in standard CMOS technology on a low-resistivity wafer, the same size as the sensor, and its readout cells are distributed in the same “pixelated” way as the sensor pixels. The merging is realized via so-called “bump bonding” or “flip-chip-bonding”. After preparing the pads with a dedicated under-bump metallization a further lithography step opens holes on each pad to place the bump metal (a), e.g. Cu or In. After removing/etching the photoresist the metal undergoes another temperature step, the so-called reflow to form balls of metal (b). The chip is then “flipped”, aligned and pressed onto the sensor, warmed up for reflow, connecting sensor channels to readout cells (c)

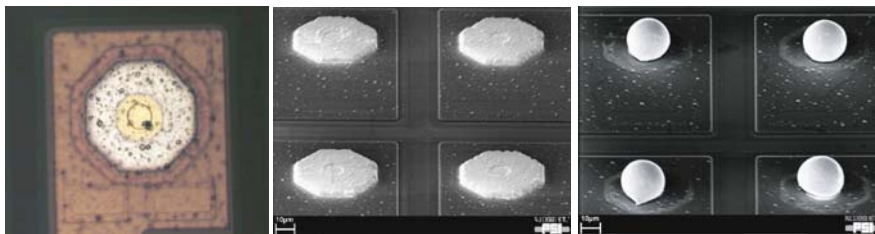


Fig. 1.64 Bump bonding at PSI for the CMS pixel detector. The *left* shows a bare contact on the pixel silicon sensor. In the *middle* part, an electron microscope picture of the structured indium bumps before the reflow process is shown. On the *right*, the bump ball after reflow is shown. The distance between bumps is $100\text{ }\mu\text{m}$, the deposited indium is $50\text{ }\mu\text{m}$ wide while the reflowed bump is only $20\text{ }\mu\text{m}$ wide [34]

LHC area full silicon pixel detectors of several barrel layers and forward disks are used in ALICE, ATLAS and CMS.

1.11.2 CMOS Detectors – Monolithic Active Pixels (MAPS)

Monolithic Complementary Metal-Oxide Semiconductor sensor or abbreviated CMOS is a pixellated sensor favourably used in industry and medical applications to detect visible light – it is on the verge of succeeding CCD sensors. It works as an ionizing particle sensor as well, as for visible light. CMOS sensors fully integrate electronics and sensor volume in one wafer, better yet there is a lower epitaxial layer serving as solid state ionization volume with standard NMOS electronics on top. The main difference to other solid state sensors used in HEP is the lack of any depletion voltage. A shallow depletion layer created purely by the pn -junction collects charges right away. Charges created in the EPI layer⁴⁷ are collected via diffusion in the N -wells. To achieve reasonable signal values, also true for light detection, EPI layers are rather “thick”, in the order of $15\text{--}20\text{ }\mu\text{m}$. The material must guarantee a long lifetime of the charge carriers to ultimately avoid trapping during the random walk. The still low signal is compensated for by very low capacitance values, hence very small noise, finally resulting in reasonable signal-to-noise values up to $S/N = 30$. The concept only works for pixels and not for strips where capacitance values are much too high. Figure 1.65 gives a cross section of a CMOS pixel cell and indicates the charge collection path. The NMOS electronic implementation directly in each pixel cell represents the first amplification step. Readout frequencies of about 40 MHz have been achieved for devices with several million pixels. The possibility of active electronic implementation directly in the sensor readout cells leads to a

⁴⁷ EPI layer: Created through epitaxy or epitaxial growth: A thin ($0.5\text{--}20\text{ }\mu\text{m}$) layer of single crystal silicon is grown over a single crystal base substrate through chemical vapour deposition (CVD). For HEP sensors thickness up to $60\text{ }\mu\text{m}$ are processed. These devices are different to the ingot growth and laser cutting described in Sect. 1.8.1.

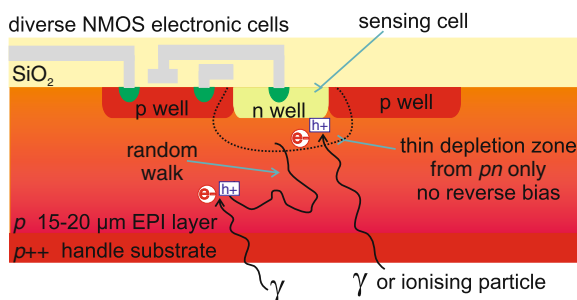


Fig. 1.65 Cross section of a CMOS sensor, one pixel. The scheme nicely depicts an example of NMOS transistors and the N-well to collect electrons from ionization or photo-effect. Electrons created inside the shallow depletion zones are fully collected while electrons from the EPI layer randomly walk towards the N-well and with an excellent lifetime behaviour only some of them will be trapped. Nevertheless, CMOS devices have an excellent signal-to-noise ratio due to their very small capacitances and low currents, therefore the low noise compensates for the low signal

large variety of detector types. In-cell amplification, shaping, storage, comparator logic, sparsification are examples, and for the future linear collider several types are listed in Sect. 6.2.

1.11.3 Silicon on Insulator Detector SOI

A relatively new technology, tested first in the SUCIMA [120] collaboration, has the potential to develop into the future star of sensor technology. The main difference between CMOS technology and fully depleted sensors is bulk resistivity and volume. A monolithic combination would be very useful. Hybrid pixels are bridging via bump bonding, both readout chip and sensor are processed separately.

In Silicon on Insulator (SOI) technology, the high resistivity, thick “sensor” silicon wafer with a SiO_2 surface will be chemically bonded to the low resistivity, thin “CMOS” silicon wafer. The processing then starts from the “CMOS” side where cavities are etched to the “sensor” part, to enable sensor side processing in a pixelated way and start CMOS processing afterwards in standard commercial IC technology. Basically it is a combination of the CMOS detectors and the hybrid pixels, as a monolithic device without bump bonding. A scheme of a SOI cell is shown in Fig. 1.66. Different to CMOS sensors SOI sensors are operated fully depleted and can accommodate NMOS and PMOS.

The basic production steps are

1. bond⁴⁸ a high resistivity (sensor-grade silicon) wafer with a low resistivity electronics grade sensor (EGS) wafer with a SiO_2 layer by thermochemical bonding of the SiO_2 parts. One is called electronics volume, the other sensor volume
2. the low resistivity silicon wafer side must be thinned down to about $1\mu\text{m}$ thickness

⁴⁸ The bonding of the two wafers is done at the SOI wafer producer.

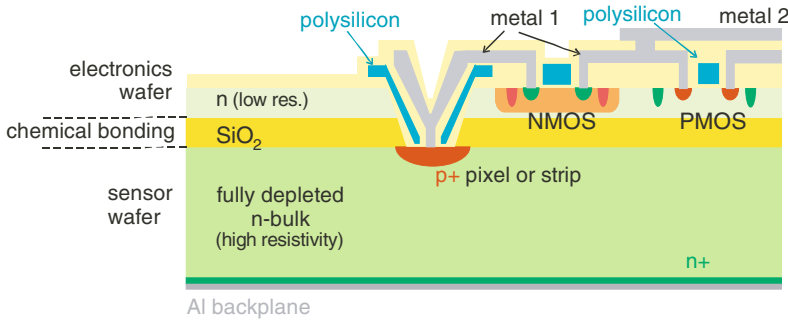


Fig. 1.66 Scheme of a silicon on insulator sensor. The scheme shows the basics of a SOI sensor. Passing charged particles create electron–holes pairs moving to the electrodes in a fully depleted high resistivity n -type sensor while the electronics are realized in a low resistivity n -type base material, separated by a layer of SiO_2 . The connection of both parts is realized by etching while the electronics processing follows standard IC methods. In difference to CMOS devices the sensor wafer can be thick, of high resistivity and depletion is possible. NMOS and PMOS transistors are possible to be processed on the electronics wafer

3. etch a cavity in the electronics volume for the later pn -junction
4. create p well on the CMOS side (later NMOS), add the $p+$ channel stopper to p well and $n+$ channel stoppers to substrate (later PMOS) (not all litho steps are listed here)
5. create pn -junction: cover CMOS part with SiO_2 , open SiO_2 between electronics and “sensor” volume, process $p+$ on “sensor”
6. apply an oxidized layer of polysilicon to protect the “sensor” side from contamination of the following processes
7. apply first metal layer, connecting pn -junction to CMOS and all necessary CMOS to CMOS connections
8. sputter SiO_2 , open CMOS contact opening and apply a second metal layer to route CMOS contacts

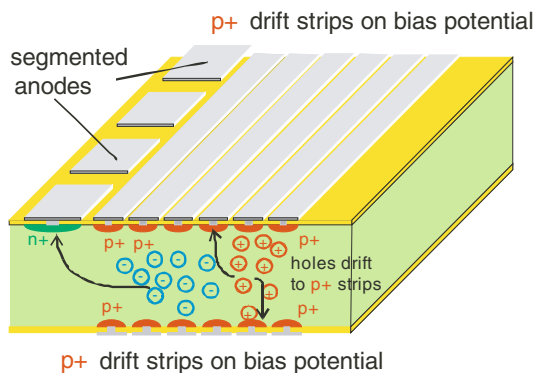
The technology is finally on the way to maturity; it is currently under discussion as a candidate for the SLHC and ILC detectors. As of today, SOI sensor technology is not HEP standard.

1.11.4 Silicon Drift Detector

Figure 1.67 shows the concept of a silicon drift detector including the drift path of the created electrons and holes. Silicon drift sensors are today used in the heavy ion experiment STAR [150] at Brookhaven [168] and will be implemented in the ALICE [90] experiment at CERN. These sensor types were first proposed in 1984 [72]. The concept is identical to gaseous drift chambers.⁴⁹ There are $p+$ strip implants on both planes of the n -type sensor plus $n+$ diode segments on the end of the sensor. A set of voltages is applied to the $p+$ strips with suitable gradient decreasing towards the

⁴⁹ Although, there is no amplification like in gas detectors.

Fig. 1.67 The concept of a silicon drift sensor. Several $p+$ strips on the same potential build a homogeneous field between sensor planes while the edge is structured with $n+$ elements where the free charge carriers drift to; the Y-coordinate is defined by the $n+$ elements while the X-position is defined by the drifting time. Depletion zone builds up horizontally



$n+$ anode. In the $n+$ implant region the charge cloud is then focussed to the anode. The Y-coordinate is measured from the anode segmentation while the X-coordinate is represented by the drift time (typically $\mu\text{s}/\text{cm}$). The homogeneity is very important and puts strict limits to the quality of the sensitive device with respect to material uniformity and small number of defects. The drift velocity needs to be predictable, therefore temperature needs to be monitored continuously and a strict calibration of the field homogeneity is necessary. The device delivers 2D information over large areas. ALICE covers $1.3\text{ m}^2 \cong 30 \times 10^6$ pixels.

1.11.5 Depleted Field Effect Transistors (DEPFET) Detectors

In contrast to all the silicon sensors previously described in this book the DEPFET sensor has an intrinsic amplification feature. The concept was proposed by J. Kemmer and G. Lutz in 1987 [99, 100]. It combines a fully depleted zone (detector bulk) and a field effect transistor (FET) (surface). When applying a negative voltage on the back the depletion grows sideways, as for the silicon drift sensors described earlier. Electrons created by a traversing ionizing particle now drift along the electrical field vs. the surface of the sensor. Different from all the other sensors, the charges are not collected directly and fed to an external charge amplifier. Electrons travel to and accumulate at the minimum potential zone formed below the gate – the so-called *internal gate*. This accumulation increases the charge density, thus increasing the FET (source–drain) current accordingly. Since the charge is not collected another active mechanism is later needed to remove it from the internal gate. Actually quite high “CLEAR” voltages in the order of 12–20 V are needed. The CLEAR voltage increases the depletion zone towards the clear contact to drain the accumulated charges. Recent developments foresee a punch through contact, which removes the charges from the internal gate – the constant clear design [111]. A schematic of a DEPFET is displayed in Fig. 1.68. A correlated double sampling can be achieved by reading the current signal before and after a CLEAR. DEPFET sensors are used in pixel design. Low noise (just a few electrons per pixel) and

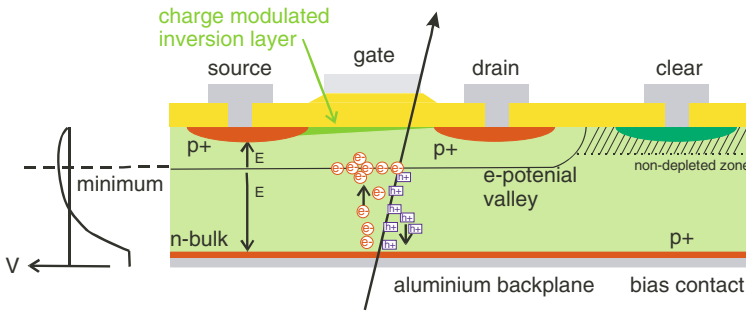


Fig. 1.68 The concept of a DEPFET sensor. The volume is depleted from the side n+ strips down to the back p+ implantation. The potential minimum of the sideways depletion is shifted towards the FET side by optimizing bias configuration. An ionizing traversing particle creates electron-hole pairs in the depleted volume. Holes are lost in the back of the device, while electrons travel to and accumulate at the potential minimum below the external GATE at the so-called internal GATE, thus increasing charge density and thus modulating *source-drain* current of the FET. The electrons stay there until actively *cleared* [111]

intrinsic amplification allow them to be thin and make them ideal candidates for tracking detectors at the future international linear collider. The missing radiation hardness prevents usage in a hadron collider, additional charges in the interfaces and bulk from radiation damage would deteriorate the FET behaviour; open channels and constant currents would be the result. Figure 1.68 depicts the first proposed version of a DEPFET detector. In today's DEPFET sensors, since deep implantation is possible, additional deep N-wells are applied to localize the electron accumulation [112]. DEPFET applications will be very probably used in the *X-ray Evolving Universe Spectrometer (XEUS)* [169] mission, in the Super-Belle upgrade as well as in the vertex detectors of the future *International Linear Collider (ILC)*.

1.11.6 3D Silicon Detectors

Initially introduced by [132], 3D sensors give a good possibility to gather enough signal from the whole sensor volume for highly irradiated sensors, even with the degradation of charge collection efficiency. In Sect. 1.10 it was shown that radiation levels of fluences of $\Phi_{eq} = 10^{15} \text{ n}_1 \text{ MeV/cm}^2$ and beyond mainly effect the charge collection efficiency and are the limiting factor of detector operation. For $\Phi_{eq} = 10^{16} \text{ n}_1 \text{ MeV/cm}^2$ a thickness above some tens of microns does not contribute anymore to the signal formation – the whole charge is trapped before reaching the electronics. The basic concept of 3D sensors is to etch pillars into the bulk and implant alternately boron and phosphorus doping via diffusion to the pillar walls or pillar filling with doped polysilicon. A scheme is displayed in Fig. 1.69. The sensors are then depleted horizontally instead of vertically thereby limiting the collection length to several tens of microns but having a substantial volume at its

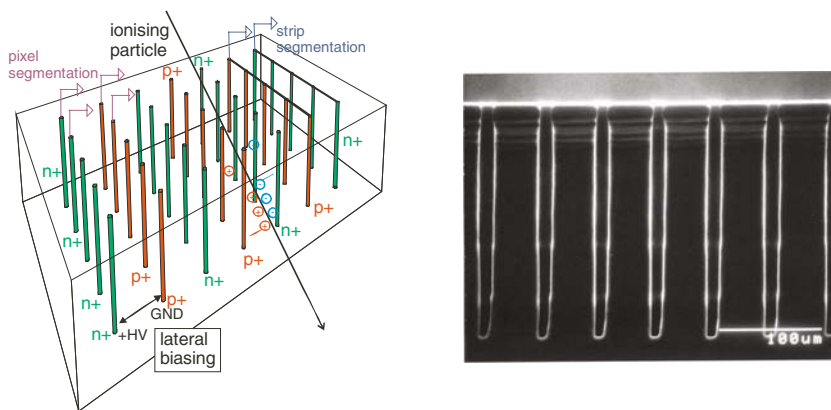


Fig. 1.69 Deviating from the standard planar sensor process deep holes are etched into the silicon to achieve holes, finally serving as electrode junctions to span the depletion zone in a horizontal way instead of the standard vertical one. The electrons and holes travel a much shorter way and are therefore less sensitive to trapping. The pillars can be combined to a strip or pixel pattern. The picture on the right shows a cut through a 3D sensor. Courtesy of CNM-IMB (CSIC), Barcelona [37]

disposal, e.g. the standard 300–500 μm . In addition the small distance between p and n pillars allows for a low depletion voltage⁵⁰ even after irradiation. The technological challenges are the deeply etched pillars. Today *Deep Reactive Ion Etching* (DRIE) (Bosch or cryogenic) is an industry standard procedure, but unfortunately it is not cheap and not available among the well-known sensor producers of HEP. Picture 1.70 shows a pillar produced with the Bosch DRIE process. The wave-like walls show clearly the alternating of etching deep down and depositing screeners (here polysilicon) to avoid a broad horizontal etch.

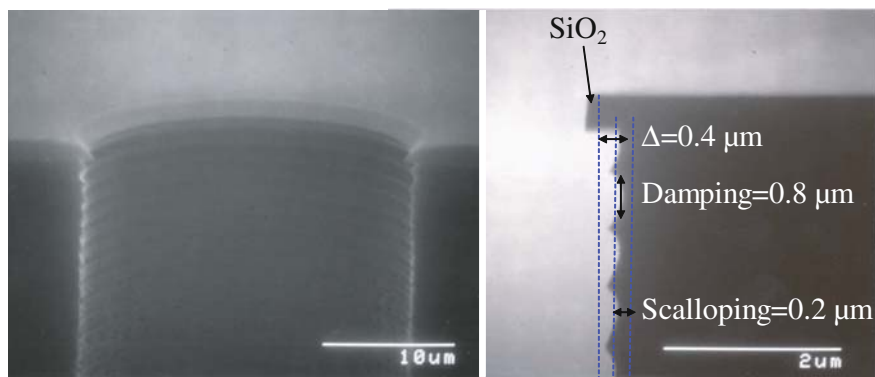


Fig. 1.70 The wave-like profile of the hole walls tells of the BOSCH etching method that was used. Frequent changes between etching and polysilicon deposit to mask from further etching ends in a deep hole with a uniform wall. The picture on the *right* shows the zoom of the one on the *left*. Courtesy of CNM-IMB (CSIC), Barcelona [37]

⁵⁰ Reminder: $V_{FD} \propto \text{distance}^2$

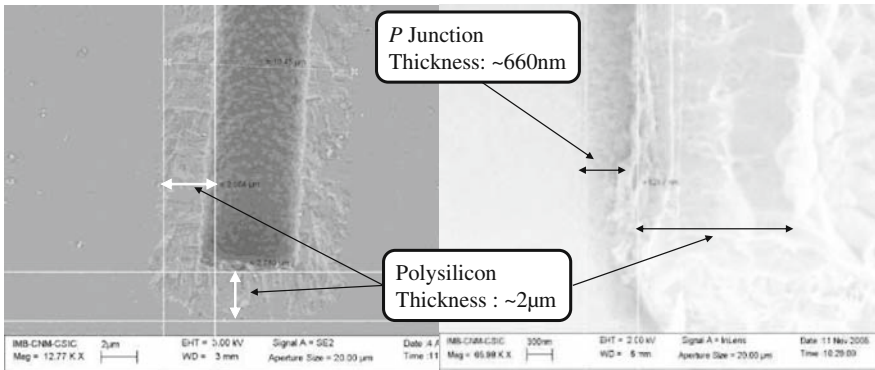


Fig. 1.71 The p and n implantation is realized via a diffusion process, the final polysilicon layers serve as protection. Courtesy of CNM-IMB (CSIC), Barcelona [37]

Diffusion processes finally implant the walls with p - or n -type dopants. This is also a two-step diffusion process, because alternating p - and n -type pillars are needed where one type of pillar is always masked, when the others are implanted. To operate the sensor, both bias voltage potentials need to be routed to the different pillars. With another scheme holes are etched from both sides into the bulk to have n -type pillar from above and p -type from below, allowing for an easier masking and final voltage connection. This two-side processing also compensates for mechanical stresses from the pillar etching. Figure 1.71 shows a length cut through a pillar with a zoom to the bottom part. The profile of polysilicon deposition and implantation is nicely visible. The main drawback is the additional etching process not compatible with the standard equipment used for planar technology. Another problem is the high capacitance load resulting in a higher noise.

1.11.7 Technology Advantage–Disadvantage – Usage

The main advantages and disadvantages of the different technology types are summarized and examples of historic, current and future usage are given in Table 1.11.

1.12 Some Last Words About the Design of Detectors for High Energy Physics

The main purpose of silicon detectors in high energy physics is the precise and efficient measurements of particle tracks without disturbance of the track itself. What are the requirements and obstacles of a real detector in a nutshell? Low mass, low noise, high signal, fast response, low power and radiation tolerance are required. Unfortunately the requirements are partly orthogonal, e.g. reduction of mass and

Table 1.11 The table summarizes the advantages and disadvantages of the main different sensor technologies. It does not claim to be exhaustive

Technology	Advantage	Disadvantage	Usage in HEP
Strip detector	Large area possible High precision ($<5\mu\text{m}$ possible) Standard processes/inexpensive Many suppliers Fast	Mostly 1D only High strip capacitance	NA11, DELPHI ALEPH, L3, OPAL CDF, D0, Belle [1] CMS, ATLAS LHCb, ALICE ILC
Hybrid pixel	2D information Standard for small r (vertex) Fast Electronics $\sim$ commercial IC	Bump bonding $\leftrightarrow$ large pixel Electronics on top (material) High channel number	DELPHI ATLAS, CMS ALICE
CCD	2D info Industry standard Thin devices possible High spatial resolution Integrated amplification	Slow Not radiation hard High power consumption Needs many different voltages	SLAC ILC(?)
DEPFET	2D Integrated amplification Low power consumption Thinning possible Low noise	Only small devices Not radiation hard High power at CLEAR Slow No industry standard	ILC(?), SBELLE?
CMOS	2D info Standard IC process Integrated amplification Low noise Thin Low power High resolution	Only small devices Short technology lifetime Small signal Only NMOS (in sensitive area) High T dependence $\leftrightarrow$ cooling	ILC(?), SBELLE?
Silicon drift	2D info Large area Standard process Double-sided process	Slow Good homogeneity needed Exact calibration necessary	STAR ALICE
3D sensor	V_{FD} independent on thickness Very radiation hard Small collection distance and time	Not yet mature (2008) No standard planar process High capacitances	SLHC(?)
SOI*	Reduction of total thickness No bump bonding necessary Electronics and sensor separated	No HEP standard	SLHC(?)

* SOI merges advantages of hybrid pixel and CMOS in a monolithic structure

radiation tolerance leads to thin detectors resulting in a low signal resulting in a low noise requirement resulting in increased power resulting in additional mass in cabling and cooling resulting in more mass.

The DELPHI detector, the largest of the LEP silicon detectors, is described in Chap. 3. Chapter 4 describes the world's largest detector in the year 2000 at the TEVATRON at Fermilab, the CDF II detector. In Chap. 5 and Sect. 6.1 examples of measures to reach an acceptable level of radiation tolerance are presented. In

Sect. 6.2 some innovative strategies are envisioned to realize a silicon detector for the *International Linear Collider (ILC)*, where radiation is low but multiple scattering is a major problem, with ultra high-precision physics planned.

1.13 Some Always Unexpected Problems Along the Way

Unlike space technology, all the HEP experiments always target for the newest possible technology. Silicon areas need to be large, sensors and electronics must be radiation resistant, space requirements are painfully tight. Only specialized companies produce sensors often in close collaboration with the HEP community. The technology is similar but also sufficiently different to standard ASIC production and light structures are preferred to very robust ones. Also high electrical fields need better material purity, well-defined doping profiles, voltage robust designs, etc. The HEP community encountered many problems along the way and this subsection gives an exemplary, but small, picture of some problems encountered in the last 20 years.

Pinholes Creation During Shipment

DELPHI, one of the LEP detectors pioneering the use of silicon microstrip and pixel sensors as vertex tracking detectors faced a mysterious sensor behaviour at its last upgrade. Perfect sensors, fully qualified at the company and subsequently delivered, showed a large number of pinholes, not at all compatible with the vendor measurement! It has to be acknowledged that measurements at these time were done manually strip by strip [12] and investigations were demanding. As a side effect, this incident led to the installation of fully automatic probe stations in the university laboratories.

It was finally identified that the plastic package of the sensor was reacting with the thermal-grown oxide thereby creating pinholes. The “flakes” caused by the “evil plastic” packaging are shown in Fig. 1.72. Because of this problem, the 1996 upgrade was partially delayed by 1 year to 1997.

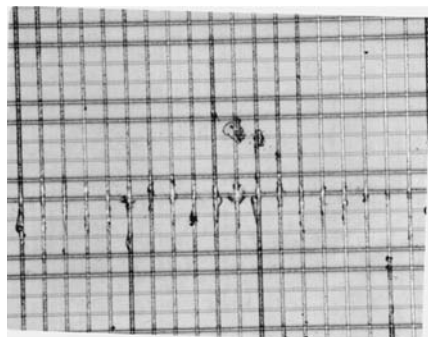


Fig. 1.72 The picture shows a “flake”, a residual substance, remaining from a plastic packaging material. The real problem was the chemical reaction with the SiO_2 coupling capacitor isolation, resulting in a short circuit between p+-implant and readout electrode, in short a pinhole

Low Inter-strip Resistance

Another incident with sensor degradation due to shipment was encountered during the CDF II sensor production. Sensors arrived at the quality control centres with regional low bias resistors and high leakage currents hinting to low inter-strip resistances. A dedicated inter-strip resistance measurement confirmed the suspicion. After some investigation the problem was spotted to be lint content in the packaging causing charge-up in the passivation oxide. Bathing in de-ionized water cured the charge-up and therefore the inter-strip resistance problem. Measurement results are shown in Fig. 1.73.

During a certain period sensors were delivered to CMS with inter-strip resistances in the order of megaohms instead of gigaohms. The dedicated process control spotted the defect on dedicated test structures. It was immediately confirmed on the large sensors. Several hundred sensors were affected and accordingly rejected. A contamination in the passivation oxide created an accumulation layer in the $Si-SiO_2$ interface beneath “short-circuiting” the strips. The failure was traced back to a small parameter variation in one machine in the production line. The inter-strip resistance history is displayed in Fig. 1.74.

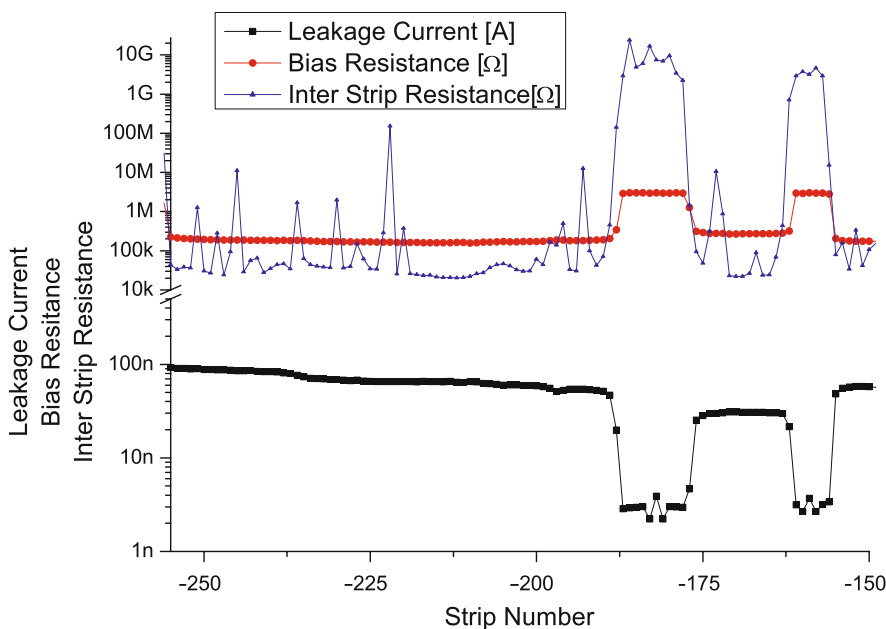


Fig. 1.73 Low inter-strip resistance after Shipping. Lint content leads to charge-up. Low inter-strip resistances were indirectly detected by leakage current plus bias resistance measurements and were confirmed by dedicated additional measurement runs [25]

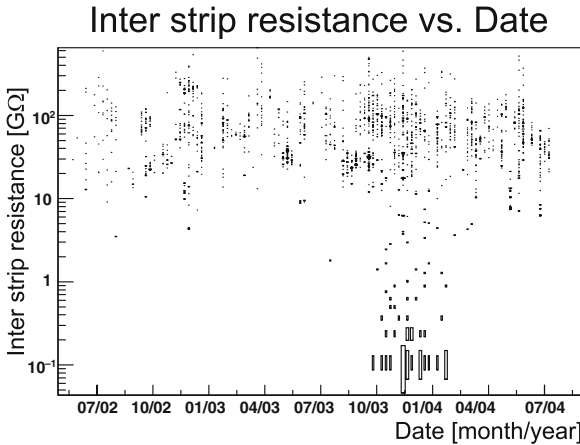


Fig. 1.74 History of inter-strip resistances of sensors delivered during 2 years for the CMS tracker. Late 2003 and early 2004 several sensor batches showed a low inter-strip resistance [25]

High Current on Isolated Strips

High leakage currents on isolated strips are a source for shot noise and in some cases with an irregular time structure due to micro-discharges, also a source of high common mode noise, affecting full chips (128 channels, see [36]). The cases in this chapter are just examples of leakage current origins and are not meant to be exhaustive. As a reminder HEP sensors are fully depleted devices with high electrical field strengths on the strip side and especially on the edges of the implants or in the CMS case on the edges of the implants and the aluminium strips (Sect. 5.1.2). This region is kind of delicate and deviations as point-like structures disturb the field configuration and can cause local breakdown. Figure 1.75 shows a CDF II example where small protrusions on the $p+$ implant strips caused a current increase from several nanoampere to several microampere. The exact defect location was identified by an IR camera finding a hot spot on the sensor.

Another prominent and severe leakage current problem was identified on the CDF II ISL double-sided sensors where one defective strip on the n -side affected a strip cluster on the p -side. A defect, a “mousebite”, in the $p+$ stops disturbed the field. The number of leaky strips on the p -side correlates to the geometric coverage of p strips to one n strip, with the 1.2° angle configuration. Figure 1.76 shows an example of a “mousebite” and the corresponding strip currents of the p - and n -side.

A prominent CMS case was superficial scratches only affecting the aluminium layer. Figure 1.77 shows examples of these scratches. Scratches were introduced during assembly but also prominently at the producer. On several sensors, the exact same scratch pattern on exactly the same strip number for many sensors was found where a pick-up tool impressed its mark [80].

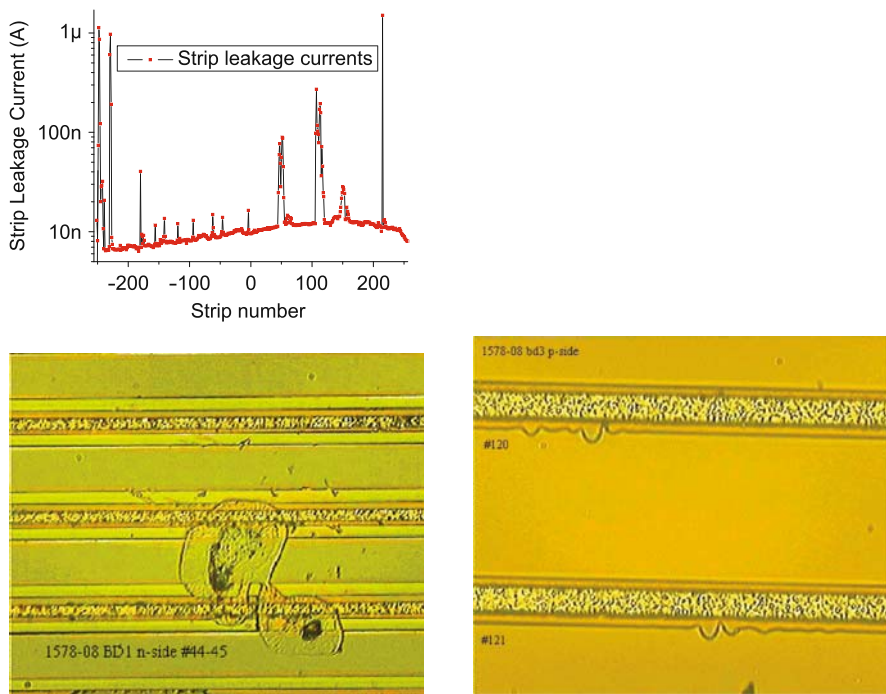


Fig. 1.75 A Single-strip fault increasing strip leakage current by 2 orders of magnitude. The small protrusion or un-regularity between the implants on the p+-side distorted the field strong enough to increase the leakage current locally. These defects often come in clusters

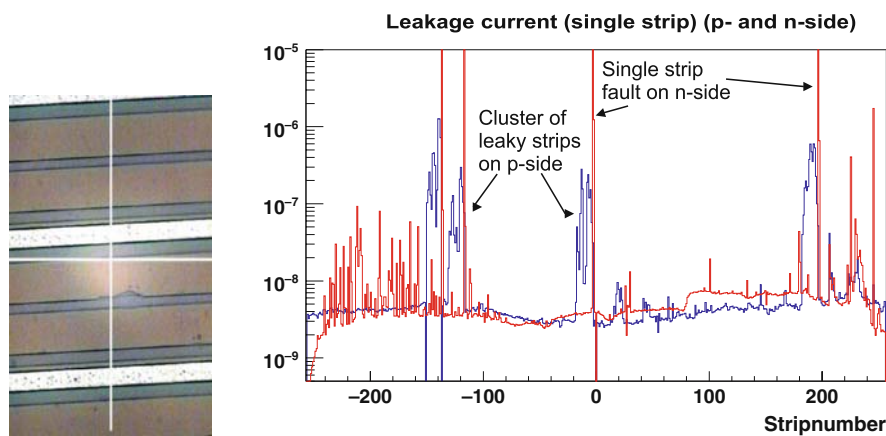


Fig. 1.76 A single-strip fault increasing strip leakage current by 2 orders of magnitude. The photo on the left shows a single-strip fault on the n-side where the p+ stop is defective. The corresponding strip currents on the n- and p-side are displayed in the right plot. The single defect affects all geometrical corresponding strips on the p-side due to the stereo layout

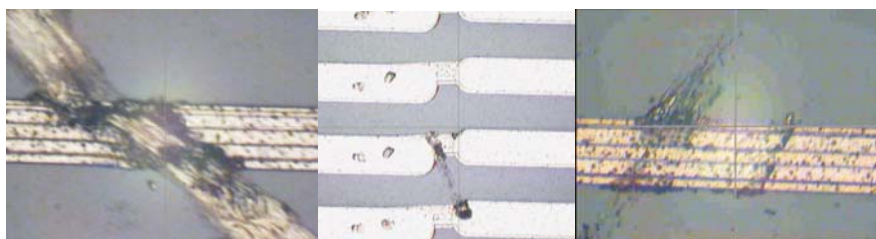


Fig. 1.77 Scratches resulting in high leakage currents. Most prominent is the scratch in the middle picture, it was present on about 50 sensors in a row, until the producer was notified. A pick-up tool was damaging the sensor with a placement precision of about 2–3 μm

Pinhole Development

With the use of charge amplifiers, direct currents are prone to saturate the preamplifiers. Pinholes, low ohmic connections from $p+$ implant to aluminium readout strip must be avoided (see Sect. 1.6.3).

During the prototype phase of the SVXII sensors, pinholes developed in the SiO_2 . In the double-sided sensors there is a net electrical field across the dielectric when bias voltage is applied. In addition wire-bonding weakened the isolation with respect to breakdown voltage. With this feedback the company was able to resolve the issue by applying a mix of “wet” and “dry” oxidation [29].

During the sensor prototyping of the CMS sensors, coupling capacitors were also weak and the number of pinholes per sensor was well above specification. Introducing an additional silicon nitride layer to the existing silicon oxide layer solved the situation.

Pinholes are sometimes optically identifiable, see Fig. 1.78. Pinholes are often “created” in final steps during shipment and also during module assembly by careless handling, thus producing deep scratches.



Fig. 1.78 Some pinholes with optical counterparts

Corrosion

During the CMS quality and process control, including long-term testing of the silicon sensors, strange stains on the guard and bias rings have been observed. The

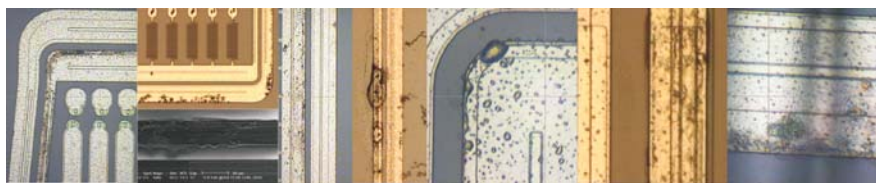


Fig. 1.79 The pictures give an optical impression of the severity of the corrosion [81]

result of a systematic investigation proved that the detectors are affected by Al_2O_3 corrosion after some time under voltage in a humid environment. Depth profiling showed that the metal structures are compromised down to the level of the SiO_2 . Finally, significant concentrations of potassium were found at precisely the location of the corrosion, serving as a catalyst for the electrochemical reaction.

Some examples of these dark-hued shades are displayed in Fig. 1.79. A full description of the incident can be found in [81]. Systematically the parameter space of time, voltage, humidity and temperature was investigated at passivated and non-passivated areas. Test duration went up to 2,000 h. Conclusive results on the necessity of voltage and humidity to drive the stain developing process were obtained. Testing at $T = -10^\circ\text{C}$ still showed a slow stain development. An electrochemical process fuelled by water, heated by electricity and catalysed by some impurities corroded the aluminium structures.

Investigating the origin of the stains, samples were submitted to an environmental scanning electron microscope (ESEM). Structural damage of the region under investigation was visible. Secondary electron emission reveals the element distribution. An atomic weight distribution of 24.31% O, 72.07% Al, 1.67% Si, 0.2% P, 0.45% S, 0.8% K was identified. By varying the primary electron energy in the

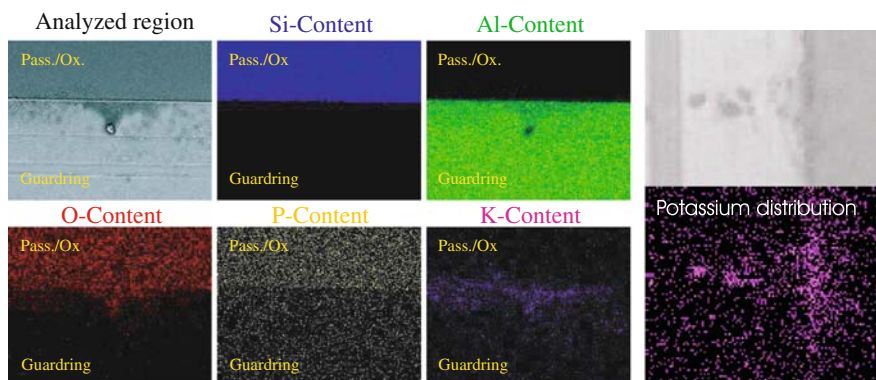


Fig. 1.80 Lateral element distribution. Comparing the optical picture with the material analysis results the missing aluminium and the abundance of oxygen catches the eye. Some spurious potassium conglomeration triggers a closer look (see *left figure*). Zooming in another region, a significant matching of potassium remnants and corroded regions is identified [81]

ESEM analysis one varies the penetration depth. In some places the same element composition was found independent of the depth. Scanning a large lateral area and recording the element content, the mismatch of Al:Si:O in the affected regions (see Fig. 1.80) becomes obvious. Examining deeply the low content impurities, such as P, S and K, a significant matching of potassium concentration in the region was identified (see zoom on the right side of Fig. 1.80). Maybe leftover potassium from a SiO₂ etching step ended up causing some undesired side effects, namely aluminium corrosion. Since potassium hydroxide is a common agent in ASIC production [121], an improper removal of acids is assumed to be the cause of the problem.

Chapter 2

First Steps with Silicon Sensors: NA11 (Proof of Principle)

2.1 From Semiconductor Detectors in the 1950s as Spectroscopes to First Tracking Devices in the 1980s

Around 1943 in the very early dawn of time, at least with respect to ionizing semiconductor nuclear detectors, P.J. Van Heerden in Utrecht¹ was concluding that a *crystal* being able to react to photons via the photoelectric effect could also be sensitive to β and α particles [85, 154]. The first tests were done with AgCl , 4 mm thick, 4 cm in diameter and γ s as reference. To establish an insulator or in the language of today, void the material of free majority charge carriers, the crystal was cooled down to low temperature in a dewar with liquid air and a high voltage was applied.

Principle of the new method. If it is possible to find substances, in which a β -particle is stopped over a short distance, while the ionization is still sufficiently strong to be measured, this would provide a means to analyze a β -radiation of small intensity. This leads to the question: what will be the ionization produced by β -rays in liquids, compressed gases and solids? "..."

In *solids* in general, the ionization current is very small, owing to the small mobility of the ions. Now the idea which underlies the present investigation is that the ionization of a single β -ray may be well-observable in a special kind of solids: namely, *crystals* that show photoelectric conductivity. Inside these crystals, light is able to free electrons which, in some of these, can move over a distance of several millimetres, if we apply an electric tension to the crystal; why should β -rays not do the same? [85, 154]

A few years later, around 1950, a germanium (Ge) detector was developed in the Bell Telephone Laboratories in Murray Hill, New Jersey, by Kenneth G. McKay [122]. In this case already a *pn*-junction was set to reverse bias to deplete the volume. Electrons and holes were collected and the resulting charge was amplified.

The number of electron-hole pairs produced in germanium by alpha-particle bombardment has been determined by collecting internally produced carriers across a reverse-biased p-n junction. "... the carriers are swept across the barrier in a time of less than 2×10^{-8} s. "... The energy lost by an alpha-particle per internally produced electron-hole pair is 3 ± 0.4 eV. [122]

¹ Mededeling uit het Fysisch Laboratorium der Rijksuniversiteit te Utrecht, Nederland.

Later, from 1955 to 1965, when monocrystalline silicon became available, *Si* detectors became a fashion, for example at the Oak Ridge and the Chalk River nuclear facilities, but also at Harwell in the UK and the CEA in France. At first simple gold surface barrier devices were constructed but within months *pn*-junctions were established by gaseous diffusion of phosphorus. The excellent energy resolution of a few electron volts predestined these semiconductor radiation detectors as miniature particle spectrometers. Still today all tracking detectors give additional energy information, where the velocity β to dE/dx dependence is described by the Bethe–Bloch formula.

The first pattern, multiple rectangular diodes on one substrate, was established in 1961 – a pixel device [51]!

The first silicon strip sensors were developed in the early 1970s in the Kernforschungszentrum Karlsruhe, the Argonne Labs, Fermilab and the Department of Nuclear Medicine in Southampton, though they were not used in high energy physics [19, 64, 77, 108]. The ones in Karlsruhe [73] (1971) for example consisted of 5 or 12 gold 3 mm wide strips, spaced by 0.2 mm, while an aluminium contact connects to analog readout. The purpose of the strips was to measure on the “large area sensor” the angle of the incident α particle from e.g. a $^{12}\text{C}(\alpha, \alpha')^{12}\text{C}$ reaction while the other electrode measured energy. The gold contacts were produced via a thin wire mask. The sensors were operated at -20°C with 30% over-depletion.

The first use of silicon sensors at CERN [23] (I found) was in 1973 where unstructured silicon was used as “live” targets where the ionization is correlated to the recoil energy. A telescope of five totally depleted silicon detectors was used as a “live” target in a coherent production experiment $\pi^- + Si \rightarrow \pi^+ \pi^- \pi^- + Si$ with a 16 GeV/c π^- beam at CERN. The active area of the detectors was 300 mm², thickness was 200 μm or 1 mm.

This section tries to assemble all relevant achievements and milestones but an overview of a lively field like early semiconductor developments cannot be complete or exhaustive.

2.2 Development of the First Silicon Strip Detector for High Energy Physics NA11 and NA32

The theoretical expectations in the 1970s for lifetimes of the lowest mass charm states were of the order of 0.1 ps corresponding to $c\tau \sim 30\mu\text{m}$ with a production cross section of a few microbarns and the charged multiplicity of hadronic interactions [68].

The requirements for a suitable detector to resolve this are

- spatial resolution: better than 10 μm and good particle separation
- rate capability about 10^6 Hz
- low multiple scattering and photon conversion – thin sensors

With their high density and small energy band gap, silicon sensors collect ~ 108 (e-h pairs)/ μm within some tens of nanoseconds collection time. Silicon is therefore perfectly suited to be used as thin and high rate detector material. The missing ingredient, very high spatial accuracy and two particle resolution, is achieved by a very fine structuring of the silicon wafer surface into a strip pattern. In the 1980s this was initially achieved by the so-called surface barrier diode method.

The surface barrier diode structure is a straightforward technique but rather delicate. After final cleaning and etching a metal (Au, Cu) strip pattern is applied to form a surface Schottky barrier junction. The pattern can be achieved by evaporation through a mask [86] or a bit more like the planar process with metal etching after applying photo-impression technique [9] as with printed circuit boards.

A new development – planar technology [92, 98] – as used in integrated circuit fabrication allowed a more robust device with higher structure precision. This technique was finally used to produce the silicon sensors for the NA11 and NA32 experiments at the SPS at CERN to identify lifetime and mass of the charm mesons $D^0(c\bar{u})$, $D^-(\bar{c}d)$, $D^+(c\bar{d})$, $D_s^+(c\bar{s})$, $D_s^-(\bar{c}s)$.

The detectors are made of high-ohmic ($3\text{ k}\Omega\text{ cm}$) n-doped silicon single crystal wafers of 2" diameter and $280\mu\text{m}$ thickness. Using the planar process, p-doped strip diodes, covered by aluminium contacts, are implanted into one side of the wafer. The sensor is DC coupled. On the other side a common aluminium contact is evaporated. The sensor is reverse biased to deplete the diodes of free charge carriers. The bias voltage also generates an electric field in the n-bulk. In order to reduce the number of electronic channels the principle of capacitive charge division has been used. Only every third (sixth) strip is equipped with an amplifier in the central (outer) region of the detector. Charges arriving at intermediate strips induce signals in the neighbouring readout strips proportional to their mutual capacitance. The strip pitch is $20\mu\text{m}$ arriving at an effective readout pitch of 60 (120) μm central (outer). The resolution was measured to be 4.5 (7.9) μm central (outer); the two particle separation was 60 (120) μm . A photo is displayed in Fig. 2.1.

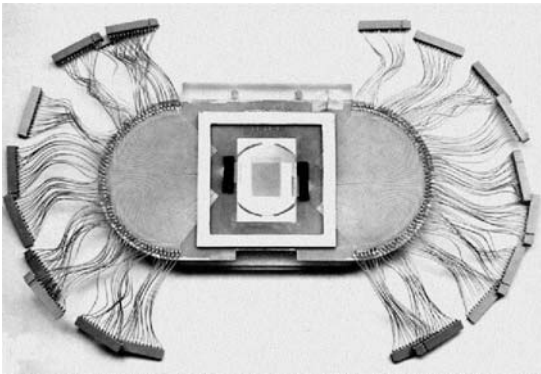


Fig. 2.1 Photograph of a mounted NA11 detector. [92, 98] The sensor seen in the center is 2436 mm^2 in size with 1200 diode strips and readout of every third (sixth in the outer region) strip, resulting in $4.5\mu\text{m}$ ($7.9\mu\text{m}$) resolution. Relaxing the readout electronic connection density to $120\mu\text{m}$ with a physical pitch of $60\mu\text{m}$ is realized by connecting the even strips on one sensor side and the odd ones on the other

Comparing the fabrication of sensors in 1980 described in [92, 98] with processing of today described in Sect. 1.8.2, it becomes clear that the planar process is still the baseline for sensor processing

1. use a $500\Omega\text{ cm} - 5\text{ k}\Omega\text{ cm}$ wafer $250\text{--}500\mu\text{m}$ thick as basis material (2 in.)
2. apply $0.2\mu\text{m}$ SiO_2 passivation at 1030°C with dry oxygen or steam leading to $1600\text{--}6000\text{ \AA}$ of SiO_2
3. open the diode windows by photolithography (SiO_2 etching)
4. use an ion implanter to get an asymmetric nearly abrupt pn -junction (ion sweep-
ing over full area, hitting only at openings)
 - for p -type strip implantation boron was used with an energy of 15 keV with a dose of $5 \times 10^{14}\text{ ions/cm}^2$
 - the backside was implanted with arsenic with an energy of 30 keV and a dose of $5 \times 10^{15}\text{ ions/cm}^2$
5. clean and thermal cure (anneal) at 600°C under dry nitrogen
6. evaporate $\sim 1\mu\text{m}$ of aluminium onto both surfaces
7. photolithographic etching of strip pattern
8. cut, mount, micro bond

In retrospect the planar technology used by J. Kemmer et al. for the NA11 experiment established some wonderful devices, the core to all current designs. Up to now there is no *real* change in the basic functionality. Especially the conclusion of [92, 98] showed a remarkable foresight:

We would like to end with the remark that high-precision silicon detectors of the type discussed in this paper have severe limitations for the use in high-energy experiments – in particular as central high-precision detectors for colliding beam experiments. For our counters the ratio of detector surface to the nearby electronics surface is approximately 1:300, which makes it impossible to cover larger areas with detectors. We think that integrating electronics on the detector chip can solve this problems.

After the intermediate step of high integration of electronics in adjacent chips (see Sect. 1.9, Chaps. 3, 4 and 5), today the direct integration of electronics on the sensors itself is a standard (see Sects. 1.11.2 and 1.11.3). Other remarks also influenced further developments, especially for the LEP era:

- detectors with readout strips on both sides to reduce multiple scattering
- large area $3''$ diameter detectors are already available
- large-scale electronics integration for amplification and data processing is needed

2.3 Distinguish c Quarks from Others

In this section the detector arrangement of NA11 and NA32 is described and the flavour tagging mechanism by the identification of a second vertex is briefly introduced. The complete NA11 spectrometer² is depicted in Fig. 2.2 [16]. This chapter

² The other detector types are listed in the figure capture of Fig. 2.2.

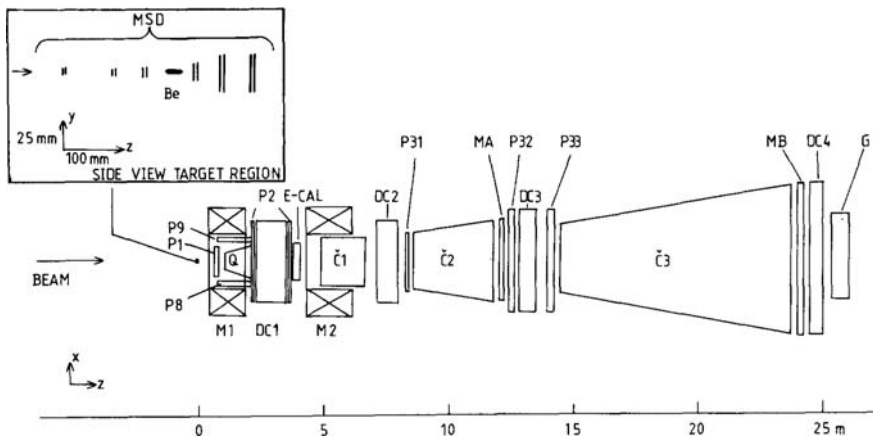


Fig. 2.2 The NA11 spectrometer. [16]. The NA spectrometer can be observed from the top. It is showing the Be target, silicon microstrip detectors (MSD), magnets (M), drift chambers (DC), Čerenkov counters (Q, Č), multiwire proportional chambers (P), scintillator arrays (MA, MB) and electron (photon) calorimeters (E-Cal, G)

concentrates on the silicon *microstrip detector* (MSD). Eight silicon strip detectors (two in front and six behind the target) of the above-described sensors were used in the NA11 and NA32³ spectrometer at CERN SPS. The detectors come in plane pairs with $\pm 14^\circ$ inclination with respect to the horizontal. The configuration can be seen in the upper left part of Fig. 2.2. The system is fully suited for a fixed target experiment. All layers are arranged perpendicularly with respect to the beam, the number of layers allows precise reconstruction, especially with the planes in front of the target defining the initial particle flight path, thus giving a good estimation of the primary vertex. The spill rate of the SPS was in the order of 10^4 – 10^6 π^- per second at 175–200 GeV/c.

The full beauty and capability of the device are revealed in Fig. 2.3. The measurement is so precise that flight paths can be reconstructed, that secondary vertices can not only be identified but the flight path of the decaying particle from its production to its decay can be quantified. Finally a handful of events showed a charm decay out of several million recorded events. The measured distance between primary and secondary vertex gives the boosted flight path $c\tau\gamma$ which is directly correlated to the lifetime of the particle. The accuracy of vertex identification is $130\mu\text{m}$. While in the case of NA11 the flight path was used to measure the lifetime, in later experiments the mere existence of a secondary vertex indicates a heavy quark. With the knowledge of the specific quark lifetime, thus flight path, the specific quark can be identified, which gives a lot of information about the full decay.

³ NA11 used a Be target, while NA32 used an active silicon target and some trigger decisions were different.

Chapter 3

The DELPHI Microvertex Detector at LEP

In the *Large Electron and Positron* (LEP) collider era, quark tagging and spectroscopy of short-lived particles demanded high-precision tracking with flavour tagging possibilities via the second vertex identification method. Taking the success of silicon sensors in NA11 (see Sect. 2.2) and MARKII [110] into account, silicon was the obvious candidate for the innermost tracking detector complemented by drift chambers and/or time projection chambers at larger radii. Therefore the first silicon vertex detectors were installed in *DEtector with Lepton, Photon and Hadron Identification* (DELPHI) [26] and ALEPH [47], with OPAL [11] and L3 [7] joining soon after.

Figure 3.1 shows the full DELPHI detector configuration with all tracking components, the solenoid, the calorimeters and the particle ID detectors. In this book the DELPHI *microvertex detector* (MVD) is described, the largest silicon detector of its time. Figure 3.2 presents a quick historical walk-through of the initial stage and first upgrades. The main part of the chapter concentrates on the last upgrade finished in 1997 for LEP2 [78, 134, 146]. Looking back on the NA11 conclusion strong efforts were made to compact the structures, especially the readout electronics and support structures, to be able to fit into the small compartment between beam pipe and the inner drift chamber. The first MVD was constrained by the beam pipe at $R = 7.8$ cm and the inner drift chamber at $R = 12$ cm; therefore, only two layers were placed at $R = 9$ cm and $R = 11$ cm.

A hint of the excitement of 1994 can be felt by looking into the internals of the DELPHI microvertex detector in Fig. 3.3.

3.1 Design and Strategies

What are the ingredients of the design and what are the requirements of high energy physics?

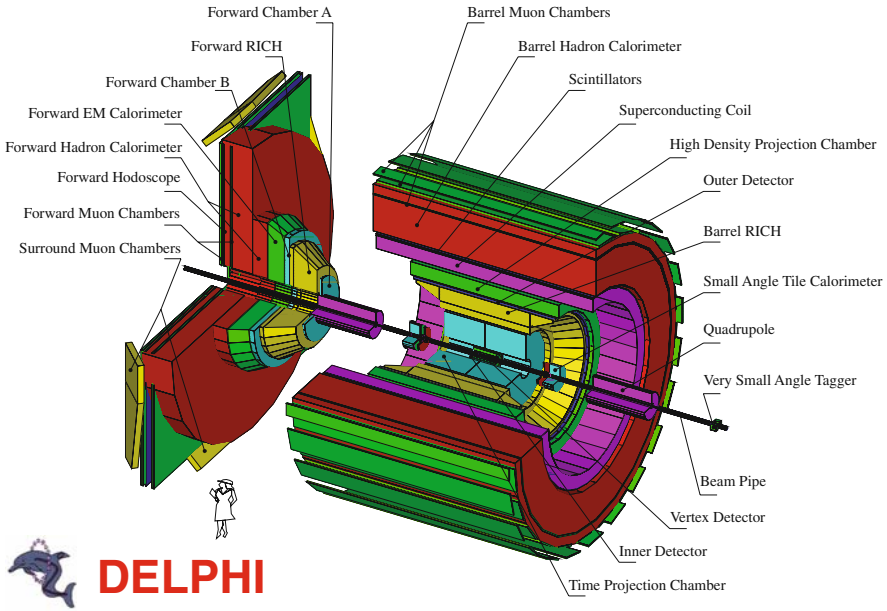


Fig. 3.1 The DELPHI detector, a schematic. The Delphi detector is a textbook example of a multipurpose detector. Arranged from inside out, the following types of detectors are illustrated: Close to the beam pipe, (1) **the microvertex detector (MVD), a silicon detector**, (2) the Inner Detector (ID), a drift chamber, (3) the Time Projection Chamber, TPC, (4) the Ring Image Čerenkov Counter, RICH, (5) the Outer Detector (OD), drift tubes, (6) the high density projection chambers, electromagnetic calorimeter, (7) the solenoid with 1.2 T, (8) Time of Flight, TOF, scintillators, (9) hadronic calorimeter, (10) muon chambers, drift chamber [Courtesy of DELPHI, CERN [54]]

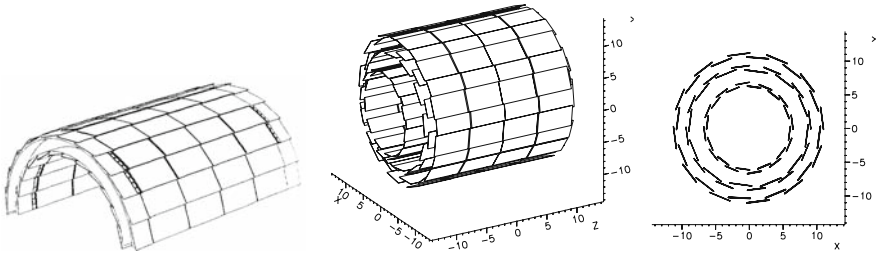


Fig. 3.2 History of the DELPHI vertex detector. DELPHI started in 1989 with two layers with single-sided readout, a R and ϕ sensitive detector as the first silicon vertex detector at LEP – a so-called $R\phi$ detector. In 1990 the beam pipe radius was reduced and a third layer, still single sided, $R\phi$ only, was introduced. Its 1994 upgrade finally contained double-sided¹ silicon sensors on three layers to establish a 3D readout of R , ϕ and z . The middle scheme shows the 3D view, while the right gives a view from the perspective as the beam particle would see it. The final upgrade in 1996/1997 is displayed in Fig. 3.4. In every upgrade sensors were reused from the former versions, due to cost effectiveness [13, 39, 115, 163]

¹ DELPHI followed the example of ALEPH, which started right away with double-sided silicon sensors.

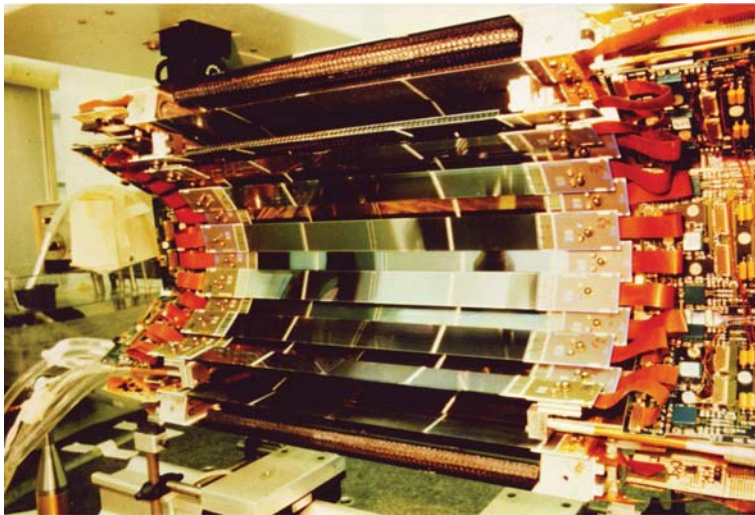


Fig. 3.3 The DELPHI silicon detector, view from within. After its first upgrade in spring 1994 the DELPHI Microvertex Detector MVD was State of the Art. The photo shows a rare view during construction, with all the modules in hand and three layers of the barrel detector assembled. The “low” number of modules allowed them to be handmarked. Compared to LHC detectors, it was quite small but the principle of geometrical module placement is still educational. The modules were placed in a so called “staggered” arrangement that the adjacent modules overlapped by a few strips. This allowed for tracks through neighbouring sensors to be used for alignment and to make sure that the whole cylinder is covered. One of the modules is detailed in Fig. 3.6 while the exploded view of the hybrid sitting at both ends of the modules is presented in Fig. 3.7

Starting from the physics point of view, secondary vertices need to be tagged mainly to identify heavy quarks² and the τ lepton to e.g. measure lifetime but equally important is to reduce background. The corresponding lifetimes are around 0.2–1.5 ps translating to flight paths $c\tau\gamma$ before decay in the millimetre regime at LEP energies. Track reconstruction must be precise enough to extrapolate back into the interaction region, resolving primary, secondary and tertiary vertices. An example of track and finally vertex reconstruction can be seen in Fig. 3.15 on page 119. The ability to reconstruct or detect secondary vertices can also be expressed by the *impact parameter resolution* σ_{d_0} . The impact parameter d_0 is defined by the shortest distance between a reconstructed track and the primary vertex, it is a crucial quality parameter of the full detector performance. If the measured impact parameter (IP) is significantly larger³ than the experimental resolution in this quantity, a secondary decay vertex is probably present. How the impact parameter is related to physics will be discussed later, this section concentrates on the detector design aspects. d_0 is dependent on the detector geometry and multiple scattering, hence the material budget obstructing the flight path. For a simplified two-layer system the variance of d_0 can be expressed by

² Heavy quarks from e.g. J/Ψ containing a c quark or the Υ meson containing $b\bar{b}$.

³ The track does *not* pass through the primary vertex.

$$\sigma_{d0}^2 = \sigma_{MS}^2 + \sigma_{geom}^2 \quad (3.1)$$

with

$$\text{with } \sigma_{geom}^2 = \left(\frac{\sigma_1 r_2}{r_2 - r_1} \right)^2 + \left(\frac{\sigma_2 r_1}{r_2 - r_1} \right)^2 \text{ and } \sigma_{MS}^2 = \sum_{j=1}^{n_{scatt}} (R_j \Delta \Theta_j)^2 \quad (3.2)$$

with σ_1 and σ_2 the intrinsic resolution in the measurement layers and $\Delta \Theta_j \simeq \frac{0.0136}{p_{\perp}^{beam} [\text{GeV}/c]} \sqrt{\frac{\Delta X}{X_0}} [1 + 0.038 \cdot \ln(\Delta X_j / X_0)]$ the average multiple scattering angle of a particle with momentum $p_{\perp}^{beam}$ traversing through the material of thickness ΔX_j (expressed in fractions of a radiation length X_0) located at radius R_j and n_{scatt} the number of layers in front of the last detection element. The IP resolution is often parameterized by $\sigma_{d0}^2 = \sigma_{asympt}^2 + \left(\frac{\sigma_{MS}}{p_{\perp}} \right)^2$ with $p_{\perp}$ in GeV/c (a fitted value derived from detector operation).

All the above considerations lead to the following design goals:

- low mass for beam pipe and vertex detector, including cables and support structures to minimize Coulomb scattering (e.g. all electronic components were placed outside the detector volume). This is especially true in front of the very first measurement layer: keeping $\Delta X_j / X_0$ and Θ_j small results in a small σ_{MS}
- placement of the first detection layer as close as possible to the primary interaction point to minimize extrapolation error, thus maximizing impact parameter resolution: r_1 small!
- largest possible radius for the outer measurement layer: r_2 large
- high intrinsic detector resolution, thus silicon sensors with small pitch and analog readout for hit interpolation in between strips: σ_1 and σ_2 small
- take alignment into account from the very beginning, thus overlap sensors to allow extrapolation of exact position with tracks crossing overlapped modules
- establish good algorithms for alignment, pattern recognition and vertex identification in the early stage

Table 3.1 Impact parameter resolution between 1989 and 2000. Initially the IP resolution was improved, then in 1994 the z-coordinate⁵ joins in and in 1997 the polar angle coverage increases from 45° to 25°. Clearly all the design criteria were rigorously followed

year	coord.	$\sigma_{Ip}^2 (\mu\text{m}^2)$	angle (°)	layer
1989	$R\Phi$	$80^2 + (120/p_{\perp})^2$	45	2
1990	$R\Phi$	$24^2 + (69/p_{\perp})^2$	45	3
1994	$R\Phi$	$20^2 + (65/p_{\perp})^2$	45	3
	Rz	$39^2 + (71/p_{\perp})^2$	45	3
1997	$R\Phi$	$28^2 + (71/p_{\perp})^2$	25	3
	Rz	$34^2 + (69/p_{\perp})^2$	25	3
1997	VFT ⁴		10.5	1

⁴ VFT: The Very Forward Tracker includes pixel and Ministrips.

⁵ Rz IP resolution is given for perpendicular tracks, since the point resolution (inclined tracks) as well as the amount of material strongly depends on Θ for the z-coordinate.

The initial detector performed superbly in lifetime measurements of the τ lepton and b -flavoured hadrons, even with only two layers and single-sided sensors allowing only $R\phi$ information. The initial aluminium beam pipe outer radius located at $R = 7.8$ cm was consequently exchanged with a beryllium one at smaller radius of $R \sim 5.5$ cm allowing for a third silicon layer at $R = 6.3$ cm in 1990. The IP resolution improved from $\sigma_{IP\phi}(1989) = \sqrt{80^2 + (120/p_{\perp})^2} \mu\text{m}$ to $\sigma_{IP\phi}(1991) = \sqrt{24^2 + (69/p_{\perp})^2} \mu\text{m}$ where the latter corresponds to $d_0 = 21 \mu\text{m}$ for a 45 GeV/c track from a $Z^0 \rightarrow \mu^+\mu^-$ decay corresponding to a point precision measurement of $8 \mu\text{m}$. The full history of measured σ_{d_0} from 1989 to 2000 is listed in Table 3.1.

3.2 The DELPHI Microvertex Detector 1996/1997

The basic necessary design features are presented in the previous section. Now what are the ingredients to cope with energies of 195 GeV/c and above for LEP2? The main design optimizations for the 1996 upgrade were driven by physics expectations like four fermion processes which ask for a large angular coverage. Also Higgs boson and supersymmetric particle searches at LEP2 were relying strongly on precise tagging of b quarks down to low polar angles. This is important to reduce W^+W^- process⁶ background. Some physics examples are described in Sect. 3.5. The MVD schematic is displayed in Fig. 3.4 while the full blossomed beauty of the microvertex

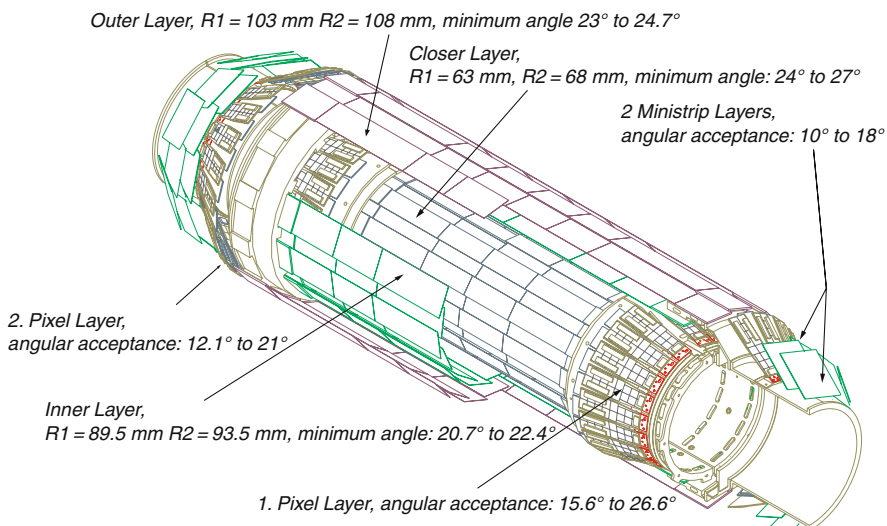


Fig. 3.4 The delphi microvertex detector [146]

⁶ The W^+W^- production cross section close to threshold energies is a few picobarns only, thus the expected event rate is relatively small and a high detection efficiency is necessary.

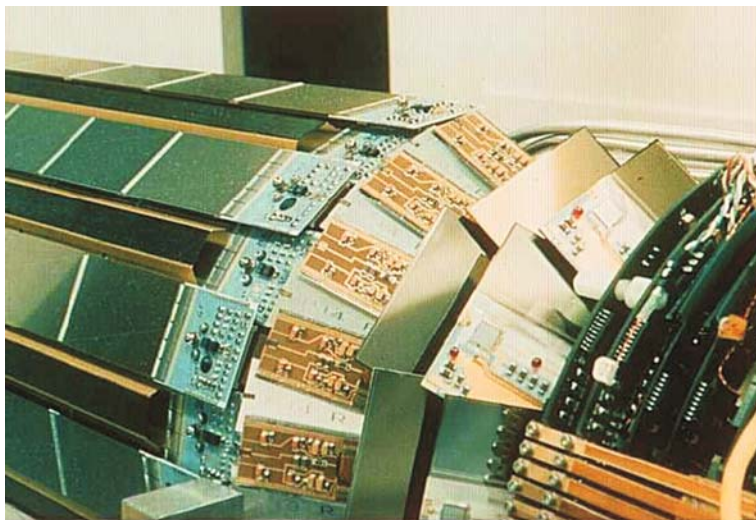


Fig. 3.5 The very forward part of the DELPHI tracker. The photo shows the forward pixel and Ministrip detector. At the time of design and construction these innovative parts enabled tracking down to $\Theta = 10.5^\circ$ [Courtesy of DELPHI, CERN]

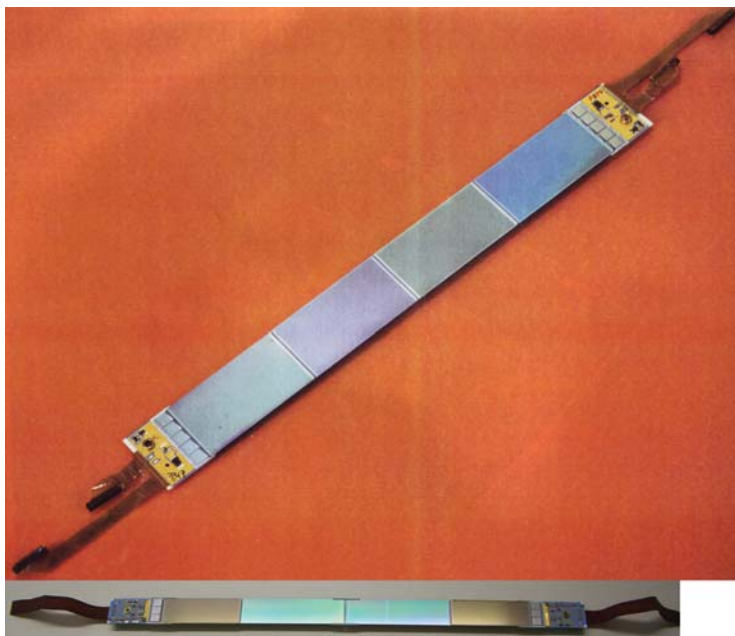


Fig. 3.6 A Delphi inner and outer module. Each hybrid reads out two detectors with the daisy-chained strips connected to each other and to the amplifiers by wire-bonding. This assembly is chosen to carefully situate the electronics outside the active volume, thereby minimizing the material budget and also minimizing multiple scattering. The outer detector module contains five chips with a total of 640 strips on each hybrid side, while the inner detector module being narrower contains only three chips with 384 strips per side

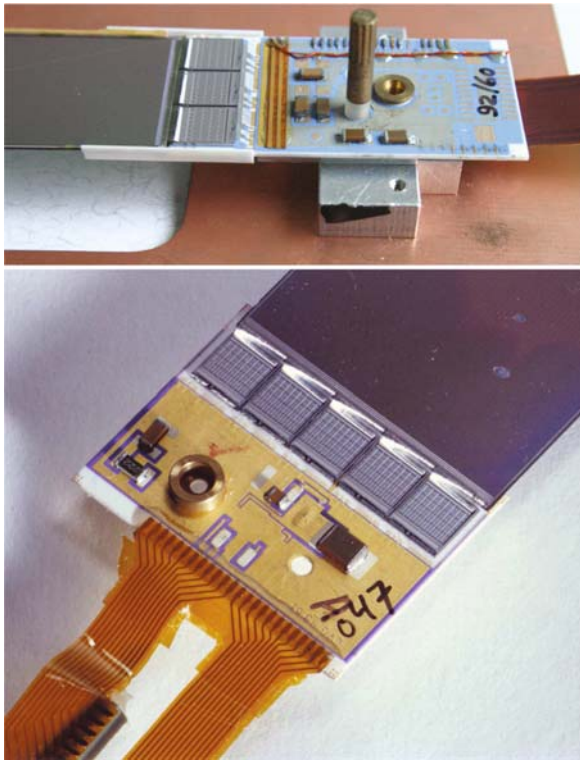
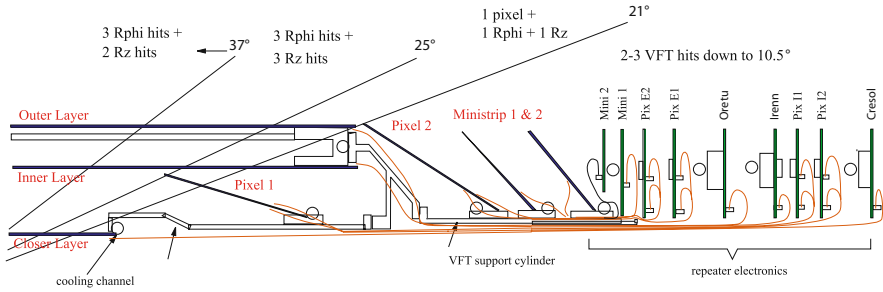


Fig. 3.7 DELPHI hybrids. Voltages and electrical signals, like clock and readout data, travel via the brown thin flex Kapton cable. Some passive components share the hybrids' space with the MX chips serving 128 channels each. The silverish connection between hybrid and sensor shows 384 (640) micro-wires. The "massive" round structure is the high-precision hole for precision mounting on the bulkhead. Notice the hand-made labels "92/60" and "A047" – the total number of modules was manageable. Without the electronics very large scale integration (VLSI) of the Microplex (MX and Triplex) chips any realization of a silicon vertex detector would have been impossible

detector is shown in Fig. 3.5. The main goal is to increase hermeticity and expand the b -tagging capabilities. These goals are met by extending the barrel region to achieve b -tagging capability down to 25° and active sensor area down to 10.5° with the additional pixel and Ministrip sensors. The three layers serve also the purpose to solve possible track ambiguities. The entire structure is 85 cm long and has 1.5 m^2 of active silicon sensors. An outer barrel module from 1994 can be seen in Fig. 3.6. The corresponding hybrids are displayed in Fig. 3.7.

The DELPHI MVD is divided into closer at $R = 6.6 \text{ cm}$, inner at $R = 9.2 \text{ cm}$ and outer layer at $R = 10.6 \text{ cm}$ tightly fitting in between the beam pipe and inner drift chamber. The *smallness* of the detector allows for many fancy solutions and very distinct optimizations. The basic concept is the usage of double-sided sensors in the closer and inner layers and back-to-back modules in the outer layers where the Coulomb scattering is less critical. The hybrids reside at the end, equipped with MX6 chips serving two sensors each in the closer layer and two or four sensors in



DELPHI

Fig. 3.8 Cross section of the DELPHI tracker – a novelty for a collider vertex detector, a forward part. DELPHI pioneered the field in two ways: (1) forward tracking and (2) usage of hybrid pixel sensors. To cope with the tight space constraints, quadratic strip sensors were mounted back-to-back with the electronics hybrid glued on top of the sensors on both sides. A single type of sensor geometry was used – the Ministrip sensor, a $53 \times 53 \text{ cm}^2$ quadratic single-sided sensor. Towards the centre DELPHI uses the new pixel technology to establish a good pattern recognition with an intrinsic 2D readout. Thin, long pixel modules just fit in this crowded region. The pixel modules reach fully into the barrel strip region [146]

the inner layer. In the outer layer one hybrid serves four sensors with the newly developed Triplex chip, optimized for larger capacitances (a short discussion on these chips can be found in Sect. 1.5 on page 29f and Sect. 1.9 on page 61f). All hybrids are double sided, having chips on both sides. In the $R\Phi$ plane the point resolution is around $8 \mu\text{m}$ and between 10 and $25 \mu\text{m}$ in the Rz plane, varying for different track inclinations. Throughout the tracker, great emphasis was placed on the overlap of sensitive silicon within each layer to allow for self-alignment procedure – a staggered design, see Fig. 3.3. The closer layer is 36 cm long, while the inner and outer barrel counts 55.5 and 55.9 cm in length. The bulkhead is constructed out of aluminium but all internal structures are lightweight Kevlar plus carbon fibre only. A minimum of water cooling runs only in the bulkhead volume.

One has to value the fact that the DELPHI vertex detector is the first one using forward structures. These are necessary to improve track extrapolation towards the forward Ring Image Čerenkov Counter, RICH, to improve Particle Identification (PID). Schematic of Fig. 3.8 expresses in detail which detector component is active in the different polar angle regions.

The detector also features the first usage of *silicon hybrid pixels* (see Sect. 1.11.1 on page 80) and rectangular strip sensors, where the hybrid is attached onto the sensor – Ministrips. These two new sensor types are elaborated upon here.

DELPHI Ministrip

The Ministrip detector consists of 48 modules arranged in two layers on the MVD bulkheads, the so-called “crowns”. Every detector is quadratic $5.3 \times 5.3 \text{ cm}^2$; therefore, two single-sided sensors can be mounted back to back with a 90° angle to

establish an intrinsic 2D readout. A Ministrip module is displayed in Fig. 3.9. The hybrids with the two MX6 readout chips are glued directly onto the sensor serving 256 strips. The strips are arranged with a stereo angle of 2° . Due to Coulomb scattering and due to unavoidable material (e.g. hybrids from the barrel modules) the resolution is anyhow limited to about $100\mu\text{m}$ and the pitch can be relaxed to $200\mu\text{m}$ with one intermediate strip. The stereo angle helps to resolve track ambiguities in the crowded forward direction. Modules of Ministrip layer 1 are reversely⁷ placed with respect to layer 2 with a resulting effective angle of 4° between strips. Two particle tracks hitting the same coordinates in one detector plane now hit, by construction, different coordinates in the second “tilted” plane.

DELPHI PIXEL

The pixel detector is formed out of 152 modules, a photo of a pixel module can be seen in Fig. 3.9. A pixel intrinsically has a 2D readout and is therefore predestined to have a marvellous pattern recognition capability and reduces any ambiguity. The modules are inclined as seen in Fig. 3.8. Each pixel module area contains 8064 pixels with a size of $320 \times 320\mu\text{m}^2$. Unlike the strip sensors (described in the next section) the pixel sensors are DC coupled and one module is read out by 16 separate chips, which have the same size as the pixels silicon sensors. The chips are aligned directly on top of the sensors and are bump bonded. A multi-layer Kapton is then glued on top of the chips to distribute control signals, power supply lines and signal lines.

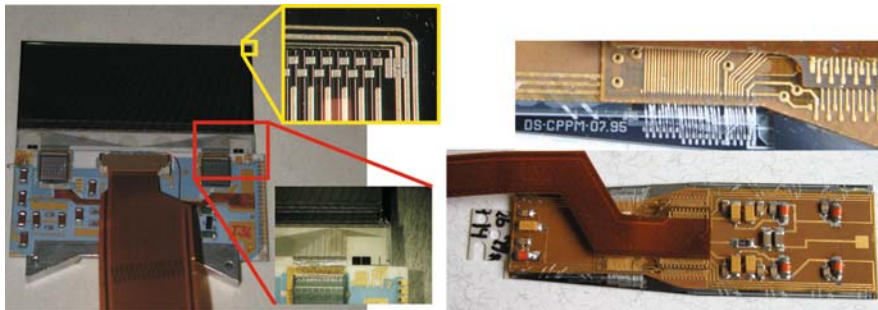


Fig. 3.9 A DELPHI ministrip and pixel module. The *left* picture shows one side of a Ministrip sensor module. The hybrid to sensor wire-bonding happened in the middle of the sensor. The sensor itself is biased via FOXFET. The FOXFET ring layout is shown in the exploded view of the sensor corner, the guard ring was connected to ground. A second zoom shows the hybrid edge including the chip edge. Two chips are sufficient for the 256 strips. The *right* picture shows a complete pixel module. The sensor-chip sandwich (bump-bonded) is covered by a Kapton flex structure carrying the necessary passive components and the bus lines. The exploded view shows the wire-bonding from pixel chip bus lines to Kapton bus lines [103]

⁷ The “horizontal” planes face each other, therefore strips are oriented $\pm 2^\circ$.

3.3 The Silicon Sensors of the DELPHI Microvertex Detector (MVD)

In the last stage of the DELPHI tracker a variety of sensors were used to first optimize in all areas and second to reuse as many sensors as possible from the older detector versions. The different sensor types, sizes and technological choices are listed in Table 3.2.

The commonalities for all the DELPHI strip sensors are the use of the *planar* technology where the implants for the *pn*-junctions were either formed by diffusion or by ion implantation. As a novelty, integrated coupling capacitors were developed for the DELPHI Microvertex detector – AC-coupled readout [35]. Different from the NA11 sensors, a dielectric layer, around 200 nm thick, was introduced between the implant strip and the aluminium readout electrode. This reduced direct currents into the readout amplifier to zero. In earlier years the different strip currents caused baseline variations of the readout and therefore required an ADC of large dynamic range. With the integrated capacitors, charges arriving at the implants are capacitively coupled to the aluminium strip. The concept is described in Sect. 1.6.3. Unfortunately a short of an integrated coupling capacitor introduces a new vulnerability to the system — pinholes. A short between implant and aluminium first allows current to flow freely to the charge amplifier and secondly disturbs the potential between chip channels, resting at a different potential than the implants. On the *n*-side of some sensors, one of these shorts resulted in a loss of about 50 neighbouring channels. The standard solution is the removal of the wire-bond but in the case of a pinhole⁸ occurring after installation,⁹ this is not a viable option. Typical values of the coupling capacitances for e.g. 7 μm wide strips are 12–15 pF/cm, sufficiently high in comparison with the strip to backplane and the inter-strip capacitance that are on the order of 0.2 pF/cm and 1–1.5 pF/cm, respectively. As mentioned earlier, $\frac{C_{\text{Coupling}}}{C_{\text{int}} + C_{\text{Back}}}$ has to be large, coupling to the readout has to dominate parasitic charge coupling. The later sensors in 1996 already used a combination of SiO_2 and Si_3N_4 layers to increase capacitance at the same dielectric thickness. The use of additional nitride also enhanced the robustness vs. pinhole creation. As a direct consequence of the additional insulator layer the necessary potential on the implants could no longer be applied via the chip channel inputs. There were two novel bias concepts applied namely, FOXFET and the use of polysilicon resistors (see also Sect. 1.3). Running at room temperature the polysilicon resistor values had to be large not to influence noise¹⁰ ($\text{ENC} \sim \sqrt{\frac{kT}{R}}$). The specification requested resistances of 5 M Ω or higher. Finally 4–20 M Ω resistors were accepted while most resistors reside well above 20 M Ω .

⁸ Noise distributions around pinholes looked like a high mountain range and the occurrence was called “Mt. Fuji”.

⁹ Fortunately, there were not too many such cases.

¹⁰ Thermal noise from parallel resistances is proportional to the shaping time, thus crucial for LEP operations. In addition the modules daisy-chain up to four sensors. The parallel arrangement of R_{poly} decreases effective resistance (see Sect. 1.5).

Table 3.2 Different silicon sensor types for different layers

	Closer	Inner	Outer	Ministrip	Pixel
Radius (cm)	6.6	9.2	10.6		
Number of modules	24	20	24	48	152
Detectors/module	4 ds	4 ds + 4 ss	R ϕ : 8, z: 8	2ss	1ss
Sensitive area (cm ²)	292	208	103	324	378
Channels/module	1536	2560	2560	512	8064
Coverage $\pm \theta$	25	21	23	10	12.2
Support	Kevlar + carbon	Kevlar + carbon	Kevlar + carbon	Al	Al
Angle to z-axis	0	0	0	49	12 and 32
Length	6.07; 7.91	5.75; 6	6	5.3	6.9
Width	2.08	3.35	3.35	5.3	1.7-2.2
Readout pitch (μ m)	R ϕ 50 z 49, 5, 99, 150	R ϕ 50 z 42, 84	R ϕ 50 z 44, 88, 176	200	330
Intermediate strips	R ϕ 1 z 0	R ϕ 1 z 0	R ϕ 1 z 0, 1	1	0
Biasing	R _{poly}	FOXFET/R _{poly}	FOXFET/R _{poly}	FOXFET	
n-side isolation	field plate	p+	-	-	-
Operating voltage	60	60	60-95	50-60	60
Readout chip	MX6	MX6	Triplex	MX6	SP8
RO channels/module	2 $\times$ 384	2 $\times$ 640	2 $\times$ 640	8064	300
Power/chip (W)	0.2	0.2	0.2	0.2	0.017

ds: double sided; ss: single sided. More detailed tables exist in [146]

The guard rings on all DELPHI sensors were connected in the *current drain configuration* and were bonded to ground, defining the electrical potential, thus electrical field, at the sensor borders. For this configuration the guard rings must surround the strip area closely, but are still located outside the bias ring.

The different choices of pitches, implant widths and aluminium widths are driven by point resolution needs ranging from 42 to 200 μm with intermediate strips for charge sharing to achieve a good resolution while keeping the number of readout channels low. Considerations, like effects of magnetic field, statistical fluctuation in the energy loss, noise performance of the electronic readout, also influenced the initial choice of thickness and pitches. The full system is small enough to allow the luxury of different parameter choices for different detector regions. The numbers are listed in Table 3.2. Along the z -axis the track incident angle increases, therefore the particle traversing paths are longer ($\cos \Theta$). For the $R\phi$ coordinates, this simply increases signal height, but for Rz coordinates with strips orthogonal to the particle path this would lead to many strips being hit, a many-strip cluster event. This is not particularly beneficial for the resolution. The signal charges are distributed over several strips thus individual strip signals are possibly too low to be significantly higher than the noise level. This problem can be circumvented by increasing the pitch along the z -axis. As an example in the outer layer, the four-sensor-long half-modules start with 50 μm pitch in the center increasing to 100 μm pitch in the second sensor and ending with 200 μm pitch for the last two sensors.

With hybrids situated at the end of the modules (see Fig. 3.6) the strips running orthogonal to the beam axis need a routing to the readout, which is realized via a second metal layer. The readout strips orthogonal to the beam axis are connected by vias at defined locations to perpendicular strips in a second metal layer. The two metal layers are separated by either a 4–5 μm thick layer of SiO_2 or of polyimide. The photo in Fig. 3.10 and the schematic in Fig. 3.11 allows us to understand the system quite well. This is true for the double-sided sensors as well as for the single-sided Rz sensors in the outer layer. An aluminium thickness of 1–2 μm guarantees a high conductivity, thus low serial noise. Unfortunately and unexpectedly in the case of the outer layer, the metal-to-metal capacitance was around 1 pF/cm and a charge loss up to 50% had to be endured [45, 78]. Operation was still possible without compromise because the charge loss was within Rz sensors where the additional charge from the longer traversing particle path ($\cos \Theta$) compensated for the effect.

In the 1994 and 1996 upgrade, double-sided sensors were introduced. In Sect. 1.6.3 on page 41 it is shown that on the n -side special precautions are necessary to guarantee strip isolation. The standard mechanism of $p+$ stops¹¹ was used – visible in the photo on the left of Fig. 3.10. In addition DELPHI used the existing aluminium readout strips above the $n+$ implants in a novel configuration. The aluminium width is wider than the width of the underlying implants. Furthermore, an appropriate potential was applied to the electrodes (negative with respect to the bulk) driving electrons away and resulting in surface depletion – the readout strips work as a gate-like electrode. With a voltage difference of 10 V and an overhang

¹¹ $p+$ stops was the common configuration; the $p+$ spray technique was developed later.

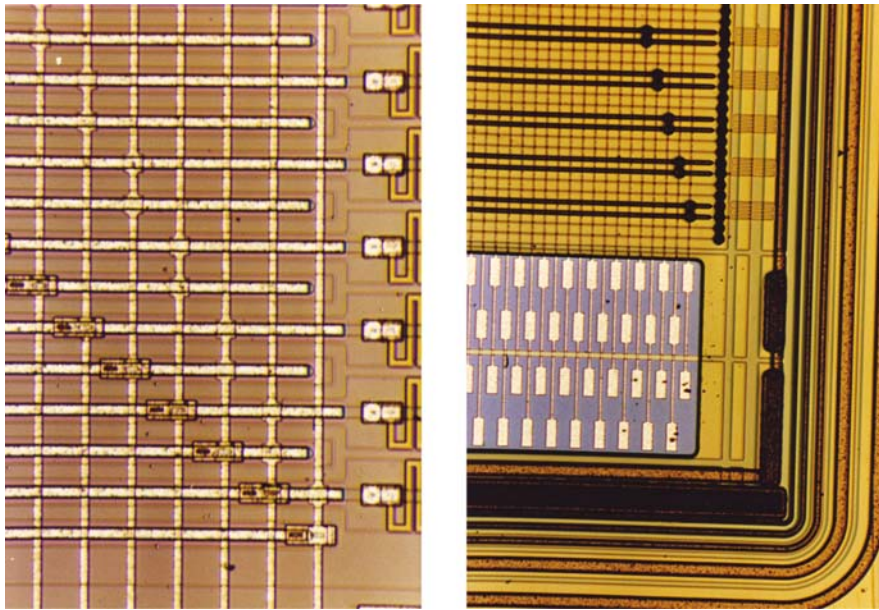


Fig. 3.10 The *left* photo shows the microscopic view of the *n*-side of a double-sided sensor. The *right* picture shows a single-sided *Rz* sensor. The perpendicular strip arrangement with the contact vias can be seen on both pictures. Both sensors are using the double metal routing to connect the strips to the readout channels. The meander structures, the polysilicon resistors, connect the bias voltage to the implants. The polysilicon length and narrow shape defines the high resistance. On the *left* picture the *n*-side structure, the *p*+ stop structures surrounding every second implant are clearly visible. They are responsible for the strip-to-strip isolation. The sensor on the *right* is also interesting; always two metal strips are connected together with two non-metallized intermediate strips (implants only) in between. With a $50\text{ }\mu\text{m}$ implant pitch, this gives $200\text{ }\mu\text{m}$ readout pitch with good charge sharing. The intermediate strips were connected to the bias ring via bias resistors on the other end of the sensor to guarantee a uniform potential on all implants. For the sensor on the *left* every single strip is connected to the readout. This gives a bit of an impression of the variety of sensors in the detector

of $4\text{--}5\text{ }\mu\text{m}$, inter-strip resistances exceeding $100\text{ M}\Omega$ were achieved – the field plate configuration.

On the other hand, a metal overhang causes possibly strong fringe fields on the edges and makes the detector potentially vulnerable to micro-discharges or the so-called “popcorn” noise. Extensive measurements were done to avoid any surprises, the onset of micro-discharge was found to be well above 90 V , thus well above the operation voltage.

Figure 3.11 presents the ultimate technology mix, a double-sided sensor with integrated coupling capacitors, serving also as field plate on the *n*-side, bias voltage supplied via polysilicon resistors and finally a double metal layer to allow perpendicular strip routing. Finally, DELPHI used the “*flip chip*” sensor module configuration. With two sensors daisy-chained, the second one is “flipped”, or in other words, the *p* strips (up) of sensor A are connected to the *n* strips (up) of sensor B. The

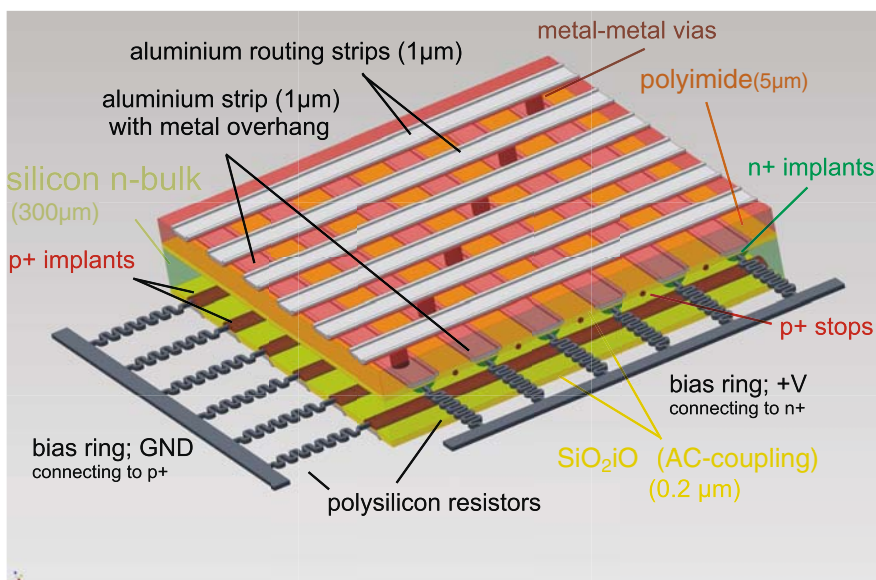


Fig. 3.11 The DELPHI double-sided, double metal sensor scheme. The sensors contain novel integrated coupling capacitors, the bias is applied via high-resistive polysilicon resistors, the n -side strips are routed via a second metal routing layer and the innovative field plate configuration guarantees $100\text{ M}\Omega$ n strip isolation

configuration is shown in Fig. 3.12 and visible in Fig. 3.6, the different reflecting colours of the sensors in the module indicate the sensor side. As a first improvement, the different noise levels of p - and n -side are balanced.¹² Secondly since p -side collects holes, while n -side collects electrons, the signals come in different polarity and therefore the polarity tells on which sensor the particle traversed, resolving ambiguities. The signals are also displayed in Fig. 3.12. This mix of technologies is applied to achieve the best possible point and impact parameter resolution and a very good pattern recognition. The effort finally paid off, when tracks like the ones shown in Fig. 3.15 could be resolved to figures like Fig. 3.18 to allow high precision particle physics in a collider experiment.

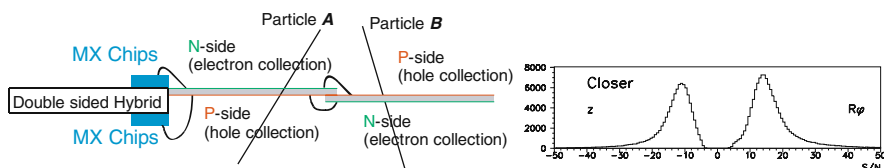


Fig. 3.12 Signals from flip module assembly. With the use of dipolar readout electronics, the signal polarity distinguishes if the particle traverses through sensor A or B of the module. Furthermore, with this connection scheme the different noise levels of n - and p -side are balanced.

¹² n -side is more noisy, e.g. due to the higher load capacitance.

Hans Dijkstra, the DELPHI Vertex Detector coordinator commented on the time of design and construction with the words:

These times were crazy, a small group of people had to deal on every corner with a new technology – new VLSI chips, beryllium hybrids, double sided sensors with integrated coupling capacitances, high precision assembly, etc. The detector was like a huge puzzle for grown-ups. We had a lot of stress and fun.

3.4 Implementation of Silicon Labs in Universities to Build a Large Device

In the LEP era, detectors became “large” and complicated, too large to be constructed at a single place. Several tasks were distributed to a number of institutes scattered over Europe. Assembly, connection and testing (quality assurance) facilities were established at many places. The right part of Fig. 3.13 shows a 3D measurement machine with a completed module under geometric survey while the left part shows the assembly jig where all modules were assembled and manually aligned. The full module construction, sensor testing, assembly (alignment and gluing), micro-wire bonding and final testing, was done at the universities. At this time the initial sensor testing was done manually strip by strip, while automatization was introduced in a later step. One famous finding of the sensor quality control is shown in Sect. 1.13. Modules were tested with laser, test pulses, β source ^{90}Sr and γ from ^{241}Am source for calibration¹³ of ADC counts to electrons.

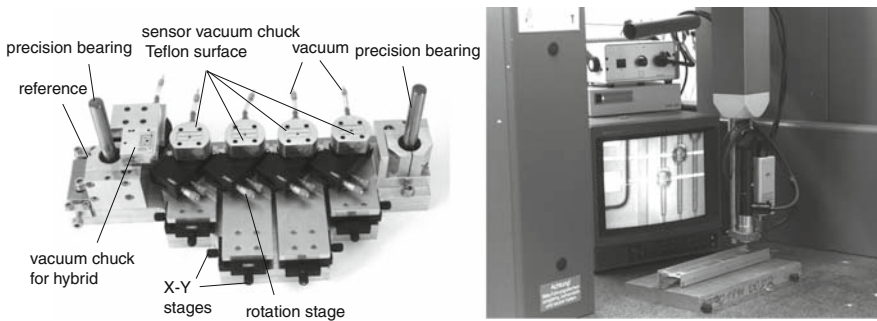


Fig. 3.13 The DELPHI assembly jig and one silicon module at final survey. The homemade assembly jig of the DELPHI outer layer modules is presented on the left. Hybrid and sensors are placed, fixed by vacuum and then positioned with the help of the 3D coordinate measurement machine. This procedure is done for the $R\Phi$ and for the R_z side separately. Then both halves were connected together with the help of the high-precision bearings. All these steps were fully manual. In a final step all modules were extensively surveyed [102]

¹³ Triggering on γ s is not possible, but with a strong source and an integration time of $2\text{ }\mu\text{s}$ a readout frequency of about 3 Hz without trigger was achieved – enough for calibration.

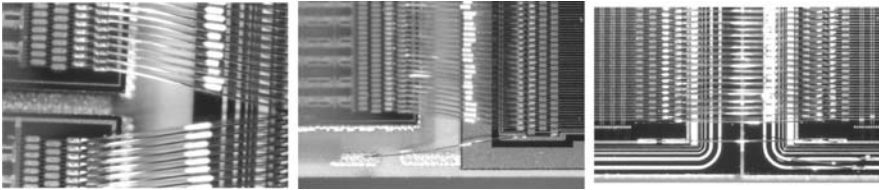


Fig. 3.14 DELPHI module bonding. The photos give an impression of the wire-bonding. The pitch is around $50\ \mu\text{m}$. The mass strip bonding was done automatically, while all special bonds, e.g. bias and guard bonds, were placed manually.

Figure 3.14 shows the fine wire-bonding of the DELPHI sensors and hybrids. As an example, one DELPHI veteran from CERN, two Ph.D. students and three undergraduates constructed 16 DELPHI outer barrel half-modules with each consisting of double-sided readout hybrids plus four+four sensors mounted back to back. Furthermore, all buses on the Kapton cables of the pixel modules were tested and all the wire-bonding for the pixels was done by students. These activities were the seeds to establish expert silicon laboratories in university institutes.

3.5 Physics with the DELPHI Microvertex Detector

This chapter lists some examples of the impact of the microvertex detectors on elementary particle physics. It is by no means meant to be exhaustive. A good description can be found in [57]. The main improvements were achieved in the

- lifetime measurements of heavy quarks and the τ lepton with unprecedented precision
- the tagging capability of heavy quarks (flavour tagging)

In addition the overall transverse momentum resolution $\sigma_{p_\perp}$ improved dramatically. The Higgs boson search during the LEP2 run was heavily supported by the vertex b -tagging capability, since a Higgs in the accessible mass range would have been coupled predominantly to $b\bar{b}$. The absence of an excess of $b\bar{b}$ events therefore established a firm lower limit of the Higgs mass.

The basic mechanism of heavy quark flavour tagging is not very different to the NA11 example shown in Fig. 2.3.

Only track points in the individual sensors, in the different barrel planes, are available. These points have to be extrapolated to tracks and good algorithms are needed to understand where the tracks start. In Fig. 3.15 a $b\bar{b}$ event exemplarily shows what the real particle paths and the initially reconstructed paths from the space points look like. The situation becomes even more ambiguous once tracking imperfections and the effects of multiple scattering are introduced. A good point resolution is necessary, because the first space points (sensor locations) are several centimetres away, while the primary to secondary vertices are in millimetre regime

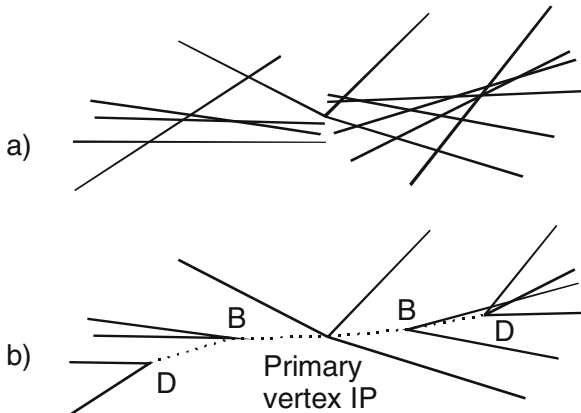


Fig. 3.15 A $b\bar{b}$ event, tracks and physics reconstruction. Two B mesons coming from the primary vertex are each decaying into a D meson, which shortly after decays into K mesons ($b \rightarrow c \rightarrow s$). A small number of tracks has to be resolved in this “simple” scenario. One should remember that tracks in silicon or also drift chambers are not continuous tracks like in bubble chambers. (a) shows the reconstructed tracks using the space point coordinate information of the silicon detectors. (b) shows the fully reconstructed $b\bar{b}$ event showing the two B mesons and their decay to D mesons, where also the different vertices are reconstructed [140]

and second to tertiary distances even less than a millimetre. However, the number of tracks not originating from the primary vertex is significant and even without full reconstruction the impact parameter d_0 delivers a good understanding of the process. Full reconstruction of all vertices from cascading D decays is therefore extremely difficult. In Fig. 3.18, a DELPHI b quark event is displayed.

Measure the Lifetime of Heavy Quarks and τ Leptons

Without quark flavour tagging the lifetime measurement of heavy quarks relies on the lepton tag, but full hadronic decays are unresolvable though having a larger branching decay ratio. Thus a larger statistical sample would increase precision. With the new vertex detectors tagging and flight path measurements the situation largely improved. The plots in Fig. 3.17 give profound evidence of this improvement. Actually two lifetime measurement methods were used.

The Impact Parameter Method

Full vertex reconstruction is not always possible. At the production threshold $b\bar{b}$ decay isotropically, as do their decay products. There is a large combinatorial background. Around 1995 the world sample of fully reconstructed B meson decays amounted to < 2000 . The additional b -tag via the impact parameter method (see also Fig. 3.16) without full reconstruction increases statistics and thus improves lifetime

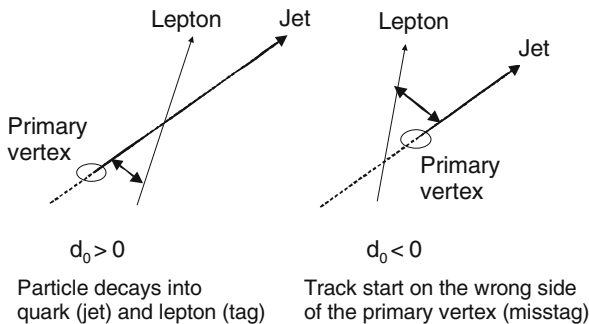


Fig. 3.16 Signed impact parameters. Particle paths not passing through the primary vertex definitively do not originate there. The impact parameter d_0 is the closest distance between track and primary vertex. The presence of a positive d_0 larger than the detector resolution therefore defines a secondary vertex and thus a lifetime tag. Negative d_0 results from detector resolution effects or a miss defined primary vertex. These signals can be used as control samples but they do not have physical significance

analysis. As described above, the impact parameter d_0 is defined by the shortest distance between a reconstructed track and the primary vertex; meaning $d_0 > 0$ defines the existence of a secondary vertex. At first order the average impact parameter d_0 is proportional to the lifetime τ_0 of the decaying particle: $\langle d_0 \rangle = \langle \beta \gamma c \tau \rangle > c \tau_0$. The first physics result obtained and published with utilizing the silicon vertex detector is the lifetime measurement of the τ lepton [5].

The Lifetime Measurement or Decay Length

The direct way to determine the lifetime, e.g. of the τ lepton, is the full reconstruction. This includes the determination of the decay path and decay length, which presents a direct lifetime measurement at known energies. Three-dimensional track points facilitate the reconstruction. Looking on the right part of Fig. 3.17, the significant improvements in lifetime measurement with the start of LEP and its silicon microvertex detectors become obvious.

Heavy Quark Tagging

Spectroscopy of particles naturally profits from a pure particle sample to obtain precision values about mass, lifetime and branching ratio. The left plot in Fig. 3.17 demonstrates the fundamental reduction of background in the $D^+ \rightarrow K\pi\pi$ decay. Flavour tagging without full reconstruction relies on the fact that the primary quarks (u, d, s) are light and have a very small probability for a secondary vertex close to the primary one. The decay products from heavy quarks with lifetimes of 10^{-13} – 10^{-12} s originate from a secondary vertex. Furthermore c quarks decay directly into

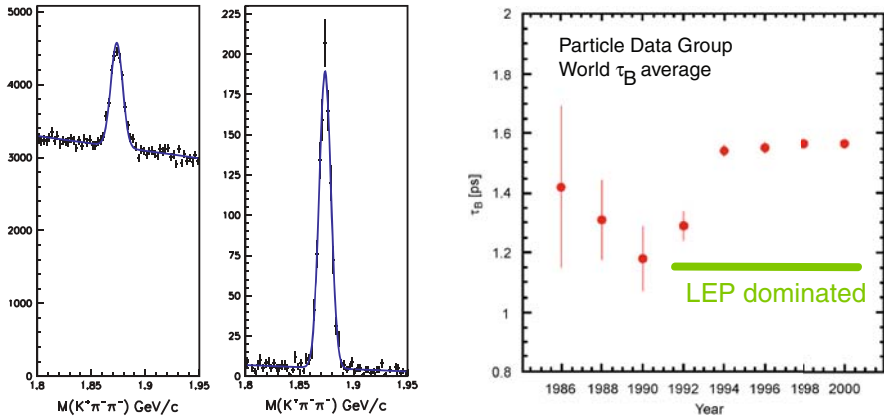
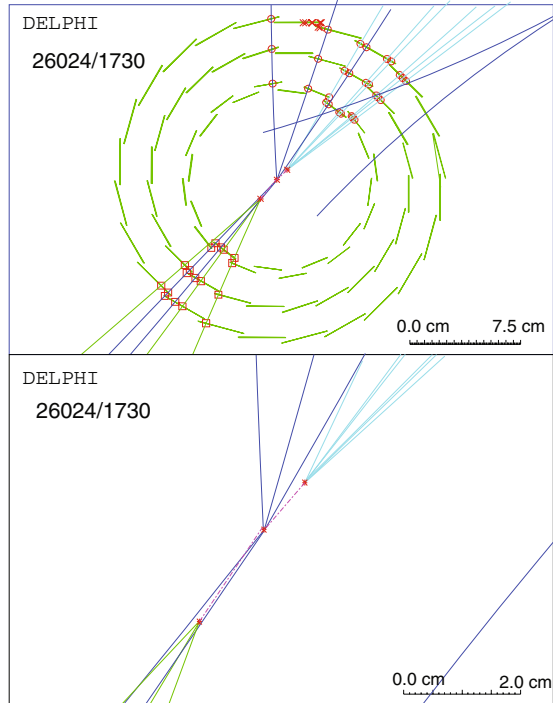


Fig. 3.17 Examples of physics potential improvement with the introduction of high-precision silicon vertex detectors in the LEP era. Plot (1) shows the $D^{*pm} \rightarrow K\pi\pi$ peak without and with 7σ vertex cut. The background suppression is impressive [89]. Plot (2) proves the clear domination of b lifetime measurement with the start of using vertex detectors at LEP. The physics results clearly support the necessity of silicon vertex detectors [46]

Fig. 3.18 A b event with the DELPHI vertex detector. The upper part of the figure displays the different track points of the three detector planes together with the reconstructed tracks. The lower part, an exploded view, shows the capability of track interpolation down to the primary vertex and to resolve the secondary b -vertex. This plot fully expresses the power of a microvertex detector to tag b quarks and determine the flight path of a short lived particle [Courtesy of DELPHI, CERN]



light quarks while b quarks decay in a cascade via c quarks to light quarks, thus producing twice as many vertices than pure c events. At the second step knowing the spectroscopic parameters, they can be used to identify/tag the decay particles which is especially interesting for cross section measurements like the determination of $F(Z^0 \rightarrow b\bar{b})$ which was limited beforehand by poor statistics. Another example is the study of jets originating from gluon radiation ($b\bar{b}g$) from b quarks by tagging the two jets from two b quarks and fixing the third jet to the radiated gluon. Figure 3.18 shows a DELPHI $b\bar{b}$ event in the vertex detector with an exploded view of the primary interaction point.

Chapter 4

CDF: The World's Largest Silicon Detector in the 20th Century; the First Silicon Detector at a Hadron Collider

The Collider Detector at Fermilab (CDF) is situated in Batavia, Illinois near Chicago. CDF is one of the two multi purpose detectors¹ at the TEVATRON proton–antiproton collider at the *Fermi National Accelerator Laboratories* (FNAL). Figure 4.1 shows the CDF detector configuration for RUN II operating since 2000 – a conventional multi purpose hadron collider detector. The beryllium beam pipe is naturally located in the centre followed by the inner tracking system consisting of three silicon sub detectors, Layer 00, SVX II and ISL, surrounded by the open cell drift chamber. The tracking volume rests completely inside the 1.41 T solenoid. The calorimeter, divided into the electromagnetic and hadronic part, is located outside of the solenoid. The drift chambers for muon detection are situated outside of the solenoid return yoke. The tracking system was largely increased for the RUN II upgrade, the silicon barrel detector's length increased to almost 2 m to cover a pseudo-rapidity² $|\eta| \leq 2$ without any endcap structure. This chapter describes solely the tracking detectors of CDF, starting with the historical evolution and focusing on the RUN II configuration.

4.1 Historical Evolution of the CDF Vertex Detector

Already at the time of NA11 and in the early design phases of DELPHI, the CDF collaboration had preliminary ideas on the use of silicon as a luminosity monitor inside the vacuum beam pipe or as forward detectors ([20, 123] 1983). The first CDF proposal of a silicon vertex detector to improve tracking resolution and to allow the tagging of heavy quarks was written up in 1985 [21]. Since the successful MX chips from the LEP experiments were tuned to low load capacitances they were not directly applicable for CDF with longer module design thus higher load capacitance. Also, bunch crossings every 3.5 μ s made pulsed powering impossible. This led 1989–1990 to the development of the first SVX chip – refer also to

¹ The second detector is called D0 for its ring location at D0 [48, 97].

² Pseudo-rapidity $\eta = -\ln(\tan\Theta/2)$ replaces the azimuthal angle Θ and is invariant vs. Lorentz addition. In hadron colliders the z-coordinate of the primary vertex varies. Therefore the quantity η is used in calculations and also to define and construct the detector elements.

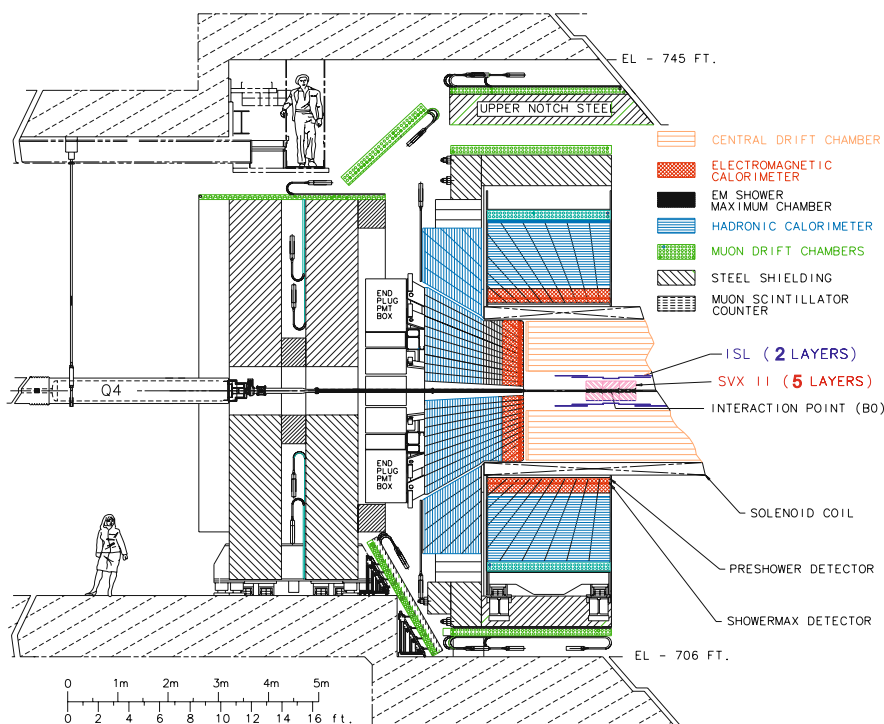


Fig. 4.1 Elevation view of half of the CDF II detector [38, 151]

Sect. 1.9 on page 61f. It contained 128 channels with double-correlated sampling and sparsification. The first chip version worked also in quadruple sampling mode since the sensors were DC coupled and the constant leakage current had to be subtracted. More radiation-tolerant chip versions with integrated ADC and optimized for shorter beam crossings followed, with later chip iterations culminating in the SVX3 chip used for the upgrade in 2000. Cooling and mechanics of the detector were constructed in Pisa and FNAL, while all hybrids and modules were assembled at Berkeley. The expertise gathered in the operation of SVX in 1992–1993 led then to the SVX', which was in operation from 1993 to 1996. The first silicon sensors were produced on 4 in. wafers with DC coupling since AC coupling had not yet matured during the design phase; it was introduced at LEP. To underline the pioneering aspect of the first vertex detector design and construction I like to cite Nicola Bacchetta:

I think the SVX was never really a formally approved project for CDF, but rather a prototype to prove the concept. Vertexing with silicon sensors was not considered viable at hadron collider. I recall vividly people being very skeptical about all the effort ... many others claiming at such radius the detector would be completely lit (100% occupied) all the time. It turned out not to be the case.

Design criteria were similar to the LEP experiments but also additional aspects are important.

- to obtain the best impact parameter resolution, a high precision point was needed as close as possible to the interaction point together with a precision link space point or better track segment to the outer drift chamber³
- in contrast to the LEP experiments in the TEVATRON, a hadron collider, the interaction region is longitudinally stretched with a σ_Z of 35 cm. This requires a long detector to cover as much as possible of the interaction
- reducing multiple scattering to the bare minimum, the material budget must be minimized
- the mechanical tolerances internally must match the intrinsic detector resolution, i.e. about $10\text{ }\mu\text{m}$, while the accurate placement with respect to the outer detector must match the resolution of the surrounding drift chamber

The SVX silicon detector (1992–1993) consisted of two barrels with four layers, single-sided, DC-coupled silicon sensors and non-radiation tolerant electronic chips, produced in $3.5\text{ }\mu\text{m}$ feature size. A full description can be found in [74] and a schematic view is shown in Fig. 4.2.

The four layers were situated at $R = 2.8, 4.3, 5.7, 7.8\text{ cm}$. Information was $R\phi$ only. The barrels stretched to a total length of 51 cm covered around 60% of all $p\bar{p}$ collisions of the TEVATRON. Three silicon microstrip sensors, 8.5 cm long and $300\text{ }\mu\text{m}$ thick, were glued on a low-weight Rohacel bar with a readout hybrid at the end forming a 25.6 cm long module/ladder. To adapt circumference differences for different layers while keeping a perfect wedge layout, the sensor widths were

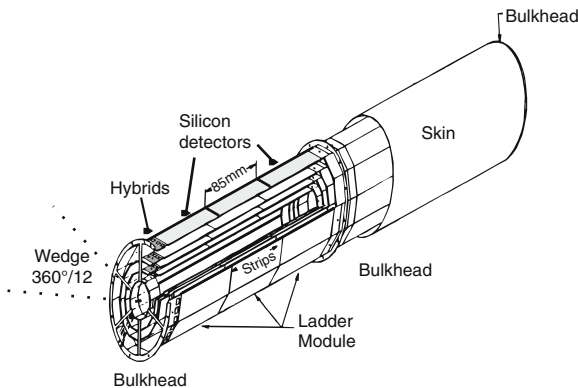


Fig. 4.2 SVX, the first vertex detector at a hadron collider, an isometric view. The consequent implementation of a wedge geometry made it necessary to have different sensor geometries per layer with different widths but same lengths. Two barrels with four layers cover 51 cm in length. Each ladder consists of three sensors with one beryllium hybrid carrying the SVX chips at the end [74]

³ CTC (Central Tracker Chamber) for RUN I and COT (Central Outer Tracker) for RUN II.

adapted. In total 96 ladders with 288 sensors were implemented. A detailed list of detector parameters is presented in Table 4.1.

Pitches of $60\text{ }\mu\text{m}$ result in point resolution of $8\text{--}10\text{ }\mu\text{m}$ and therefore an impact parameter resolution of $\sigma_{IP_\phi} = \sqrt{13^2 + (39/p_\perp)^2}\text{ }\mu\text{m}$. Typical flight path lengths D are on the order of $350\text{ }\mu\text{m}$. It was then possible to resolve B -decays which was a major success. Cuts on decay lengths improved invariant mass measurements greatly.

After around 30 pb^{-1} of data between 1992 and 1993 in RUN Ia with around 30 krad of radiation, the increase in sensor leakage current saturated the preamplifier and in addition significant threshold changes in the transistors deteriorated gain and increased noise.

The basic geometric parameters for SVX and SVX' are comparable to those in Table 4.1, just layer 0 was moved 2 mm closer towards the beam pipe. The main improvements were the technology choices of electronic chips and sensors. The new chip SVXH being produced in $1.2\text{ }\mu\text{m}$ technology was radiation tolerant up to 1 Mrad. It also featured higher gain with less noise and contained an 8-bit ADC on chip. The sensors contained integrated coupling capacitors to avoid dark current into the chip which therefore was operated in double-correlated sampling instead of in quadruple mode. The SVX' detector was successfully operated from 1992 to 1996. During this time algorithms were already developed to have a silicon standalone tracking. As in DELPHI basically all sensors and modules were different for each layer which gives the detector the predicate to be a “work of art”. During operation, the detector had an efficiency of $>99\%$ with an average position resolution of $\sim 12\text{ }\mu\text{m}$ and an asymptotic impact parameter resolution of $13\text{ }\mu\text{m}$.

The silicon upgrade for RUN II is described in detail in the next section but first design considerations are given here – the lessons learned from the SVX and SVX'. The longer shutdown between RUN I and RUN II made a major upgrade possible. Also with the success of SVX and SVX' the project was more fundamentally supported. The design parameters were defined by the need for a large coverage, a good impact parameter d_0 and transverse momentum $p_\perp$ resolution.

The transverse momentum resolution $p_\perp$ is defined by

$$\frac{\Delta p_\perp}{p_\perp} \approx \frac{\Delta s[\mu\text{m}]}{(L[\text{cm}])^2 B[\text{T}]} p_\perp [\text{GeV}] \quad (4.1)$$

Table 4.1 Design parameters of the SVX detector in CDF at the TEVATRON, the first silicon vertex detector in a hadron collider experiment

	Width [μm]	Pitch [μm]	Number of strips	Number of chips	Sensor/layer length [cm]	At radius [cm]	$\eta \pm$ coverage
Layer 1	15.3	60	256	2	8.5/25.6	2.8	2.9
Layer 2	23	60	384	3	8.5/25.6	4.3	2.5
Layer 3	30	60	512	4	8.5/25.6	5.7	2.2
Layer 4	42.2	110	384	3	8.5/25.6	7.8	1.9

The detailed parameters are presented for the SVX from the conceptional point of view. There were no real changes towards the SVX' detector with respect to part numbers of geometric placements. Of course, there have been significant changes in the silicon and chip technology.

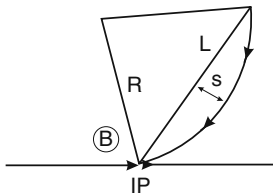


Fig. 4.3 Transverse momentum resolution $p_{\perp}$. The momentum resolution of a moving charged particle in a B field is given by its curvature path. With $s = L^2/8R$ and $B \cdot R = p/q$ one gets the momentum resolution as $\frac{\Delta p}{p} \approx \frac{\Delta s}{L^2 B} p$

with sagitta $s = L^2/8R$, lever arm L , magnetic field B , curvature radius R and momentum $p_{\perp}$. The equation immediately tells that (a) intrinsic position resolution has to be good to resolve s and that (b) the B field strength gives a linear improvement, while (c) a larger lever arm improves momentum resolution quadratically. An explanatory scheme is given in Fig. 4.3. With increasing $p_{\perp}$ the resolution gets worse again and with an error of 100% not even the charge of the particle can be identified anymore.

A layer around $R = 20$ cm was necessary to improve σ_{d_0} and $p_{\perp}$ resolution. The short lever arm of 5 cm realized in the SVX' detector resulted in a poor $p_{\perp}$ resolution and the track extrapolation to the drift chambers was not precise. An overall increase in length was needed to increase coverage. This led initially to a five layer SVX II detector with layer 4⁴ at $R = 10.6$ cm. The length of SVX II was increased to 96 cm by adding a third barrel. To improve pattern recognition and allow for a 3D vertex reconstruction double-sided, double metal silicon sensors were introduced. To bridge between vertex and drift chambers an *Intermediate Fibre Tracker* (IFT) or an *Intermediate Straw Tracker* (IST) was proposed. Both concepts suffered from the necessary extensive R&D in the short available time period. Both were finally cancelled and additional *Intermediate Silicon Layers* were introduced, the ISL detector. To make it affordable, a large fraction of the sensors were produced on 6 in. wafers⁵ – the first time for HEP experiments. The only remaining flaw in the concept of this beautiful detector is the unavoidable amount of material disturbing the impact parameter resolution, thus the b -tagging capability. This was solved by adding even more material but at a very low radius, namely adding a layer 00 at $R = 1.6$ cm directly onto the beam pipe. The closer space point recovers σ_{d_0} for the latter multiple scattering, refer to formula (3.1).

With an expected integrated luminosity of 2 fb^{-1} the front electronics radiation tolerance needed to be improved. This led to a third generation of the SVX chip series – the SVX3 chip (Sects. 1.9 and 4.2.1). Somehow the SVX detector noise increased above expectation during RUN Ib and this was attributed to the FOXFET

⁴ Layer 4 is the fifth layer, since counting starts at layer 0 with an additional layer 00 further in and the outer ISL layer count starts at 6.

⁵ The 6 in. wafer contained two sensors in one processing step.

biasing, being less radiation tolerant than anticipated. As a result for RUN II polysilicon bias resistors were introduced. Last but definitely not least the SVX II information was introduced into the Level 2 trigger – the CDF Secondary Vertex Trigger (SVT).

4.2 Design, How to Cover $|\eta| \leq 2$ Without Endcap

In 2000 the TEVATRON was upgraded for RUN II to higher luminosity and a slightly higher energy 1.8 TeV to 2 TeV. The corresponding tracking system is described in detail in this section.

4.2.1 Tracking System

Efficient precision charged particle tracking is extremely important for the CDF analysis technique. Reconstruction of both high $p_{\perp}$ (m_W) and low $p_{\perp}$ ($B \rightarrow J/\Psi K$) is required. The combination of track, calorimeter and muon chamber information, with an excellent purity at both the trigger and offline level, is possible. Precise and efficient b tagging is essential for top physics and new phenomena searches. The goal is to guarantee precise 3D impact parameter resolution with an enhanced coverage up to $|\eta| \leq 2$. The CDF II tracking system consists of an inner silicon vertex tracking system and a large drift chamber. The inner tracker consists of a minimum radius inner layer (layer 00 at 1.35 cm) glued to the beam pipe and a five-layer silicon detector (SVX II at $R = 2.7$ – 10.7 cm) with two-dimensional readout in each layer. It is surrounded by a third two-layer silicon detector (ISL $R = 20$ and 28 cm) and finally an eight-layer open cell drift chamber (Central Outer Tracker (COT) at $R = 44$ – 132 cm). It is worth mentioning that the $|\eta| \leq 2$ coverage was achieved with a consequent long barrel geometry and without any forward structures. Layer 00 and SVX II are ~ 1 m long, the ISL spans even ~ 2 m.

The full tracking volume can be seen in Figs. 4.4 and 4.5, the latter giving an expanded view of the inner part. The inner and outer tracking systems are capable of standalone tracking. This enables track–track matching instead of the normal track space point fit. The COT gives level-1 trigger information and the inner silicon tracking system provides level-2 information. The trigger acts on displaced vertices.

Layer 00

With a silicon layer placed at very small radius, the first precision space point is recorded without earlier multiple scattering thus improving impact parameter resolution. A 6-wedge layer is mounted directly on the beryllium beam pipe with single sided-silicon microstrip sensors, each being 7.8 cm long and 0.8 cm or 1.5 cm wide.

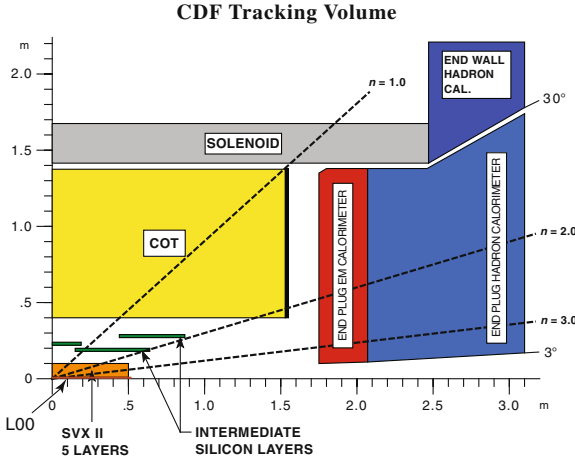


Fig. 4.4 Longitudinal view of the CDF II tracking system [142]

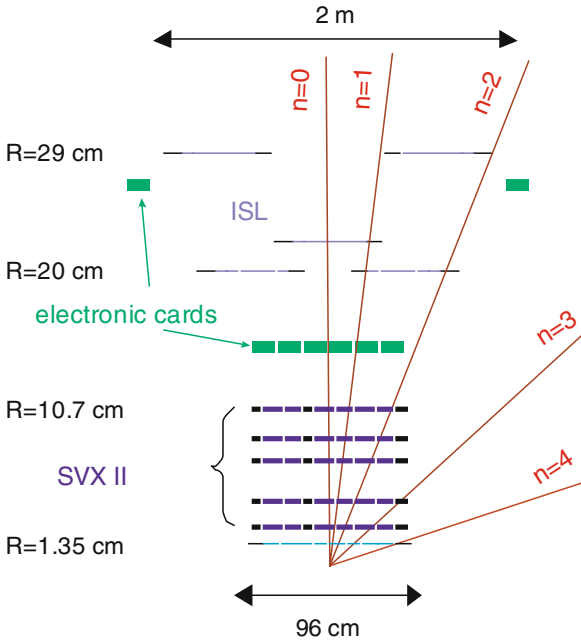


Fig. 4.5 CDF silicon tracking system. Full tracking is possible up to $|\eta| \leq 2$ [142]

The length of layer 00 is approximately 94 cm, consisting of six modules with two sensors per module, summing up to a total of 144 sensors. Sensors are placed at $R = 1.35$ cm and $R = 1.6$ cm (see Figs. 4.5 and 4.6).

The caveat of a very high radiation environment is overcome by using radiation hard silicon sensors following early design recipes of the freshly developed LHC

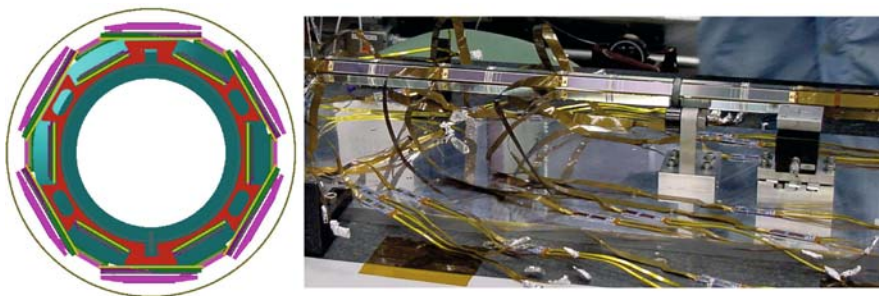


Fig. 4.6 End view of the layer 00 detector and a rare view during assembly. The left side expresses the tightness, allowing only 0.8 cm (1.5 cm) wide sensors at a radius of 1.35 cm (1.6 cm). Layer 0 of the SVX II detector sits already at $R = 2.45$ cm. On the right layer 00 is visible with silicon sensors not yet covered by the thin long fine-pitch cables. The main importance of layer 00 is the first high precision space point at very low radius to seed the impact parameter calculation before multiple scattering [93]

sensors and silicon material proposed by the RD50 collaboration. The sensors were single-sided only with p-on-n $R\phi$ readout. They were produced on $\langle 100 \rangle$, 300 μm thick silicon, AC coupled with a multi-guard ring structure to guarantee high voltage operation, which is the key to radiation-tolerant operation. Some sensors were even oxygenated (see Sect. 1.10.1). Strip implants were spaced 25 μm while every second strip is connected to the readout. The sensors are actively cooled to freeze radiation damage and reduce leakage currents.

The radiation-tolerant SVX3 chips are mounted along the line separated from the sensors by longer cables at larger radii. Signals are carried out by thin, fine-pitch cables up to a length of 47 cm. Free cables can be seen in Fig. 4.6 while final assembly of layer 00 during insertion with cables strapped tightly together is displayed in Fig. 4.7.

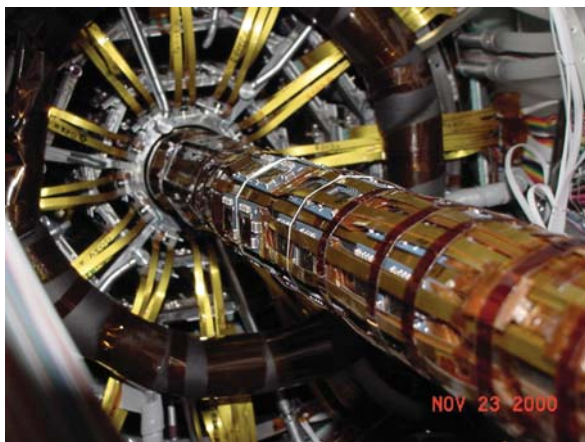


Fig. 4.7 Layer 00 during insertion. The clearance towards the SVX II detector is about 300 μm only. Insertion finally succeeded in November 2000 [93]

Table 4.2 Parameters of the CDF II Silicon Sensors, SVX II, ISL and Layer 00. The large variety of silicon sensor types gives an impression about the complexity of the device. Only the large area outer ISL detector is fabricated with a single sensor type

Sensor parameters	Layer 00		SVX				ISL	
	Layer 00	Layer 0	Layer 1	Layer 2	Layer 3	Layer 4	ISL L6 (4 in.)	ISL L7 (6 in.)
Radial distance (cm)	1.35/1.6	2.45	4.67	7.02	8.72	10.6	19.7/20.2 F	28.6/29
Stereo angle (degrees)	–	90	90	+1.2	90	–1.2	22.6/23.1 C	1.2
$R\phi/z$ readout channels	128/256	256/512	384/576	640/640	768/512	896/896	512	512
$R\phi/z$ readout chips	1/2	2/2	3/3	5/5	6/4	7/7	4/4	4/4
$R\phi/z$ strip pitch	(μm)	60/141	62/125.5	50/60	60/141	65/65	112/112	112/112
Total width (mm)	0.85/1.48	17.14	25.59	40.30	47.86	60.17	59.3	59.3
Total length (mm)	7.84/7.84	74.3	74.3	74.3	74.3	74.3	69	74.8

A summary of parameters is given in Table 4.2. The layer 00 was proposed very late as a “beyond baseline” detector component, a detailed description of the early idea can be found in [113, 127].

Silicon Vertex Detector (SVX II)

The SVX II is divided into 12 wedges in $R\phi$ and in 3 barrels in z (beam axis) with a length of 29 cm each. This results in a total length of 96 cm, almost twice as long as the former SVX or SVX'. With the length of almost 1 m SVX II covers $\approx 2.5\sigma$ of the interaction region providing track information up to $|\eta| \leq 2$. It has five double-sided silicon layers measuring the $R\phi$ and Rz coordinates. Three layers (0, 1 and 3) have a 90° stereo angle allowing high-resolution Rz measurements, while layers 2 and 4 have a 1.2° stereo angle. This design provides good pattern recognition and 3D vertex reconstruction with an impact parameter resolution $\sigma_\phi < 30\mu\text{m}$ and $\sigma_z < 60\mu\text{m}$ for central high momentum tracks. Figures 4.4 and 4.5 show the location of the SVX II detector and the ISL. The SVX II replaces the former SVX – a four-layer, single-sided silicon microstrip detector. A photo of one SVX II barrel is displayed in Fig. 4.8. Half-ladders contain two sensors plus a hybrid mounted directly to the

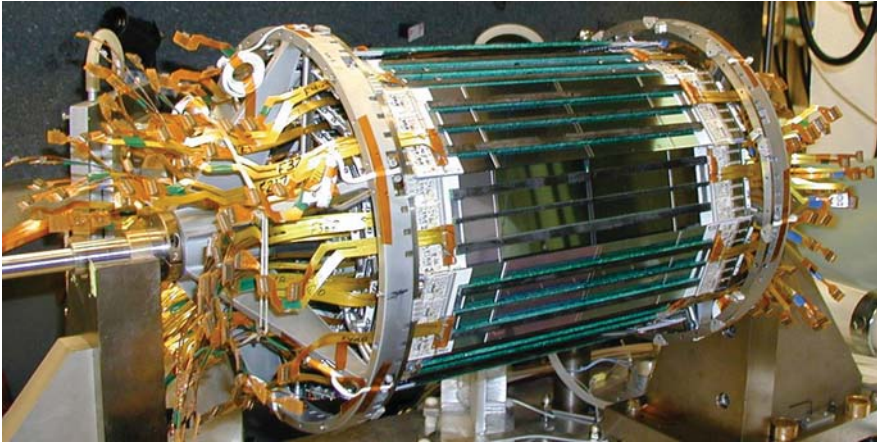


Fig. 4.8 The SVX II detector, one barrel [27]

silicon surface at the end. Two half-ladders are daisy-chained together to form full ladders of four sensors each. A total of 720 sensors form 360 half-ladders or 180 full ladders. A photo of an SVX II module is presented in Fig. 4.9.

A 12-fold ϕ symmetry makes it possible to treat each 30° wedge as an independent tracker. As for the SVX, the sensor widths had to be adapted for each layer to make a perfect wedge geometry possible. The data from SVX II are used at the level 2 Silicon Vertex Trigger (SVT) [124], which identifies displaced vertices coming from B fragmentation. A placement precision of better than $100\ \mu\text{m}$ with respect to the beam was necessary to use track information in the Level 2 trigger.

All SVX II sensors are AC coupled, double sided, $300\ \mu\text{m}$ thick with polysilicon bias resistors. The $R\phi$ side contains the p -implants, while the Rz or stereo side is composed of n -implants isolated by a p -stop configuration (see also Fig. 4.17). For the 90° Rz strips, a double metal layer routes the signals to the readout electronics. A photo of the double-sided sensor layout is given in Fig. 4.10. For the small stereo angle sensors no extra routing is needed. In Fig. 4.17 one can see how layer 2 and layer 4 sensors are processed on a single wafer with the new 6 in. sensor

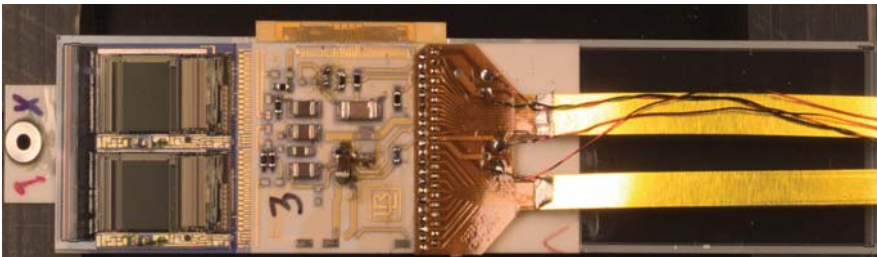


Fig. 4.9 A layer 1 hybrid with sensor [27]

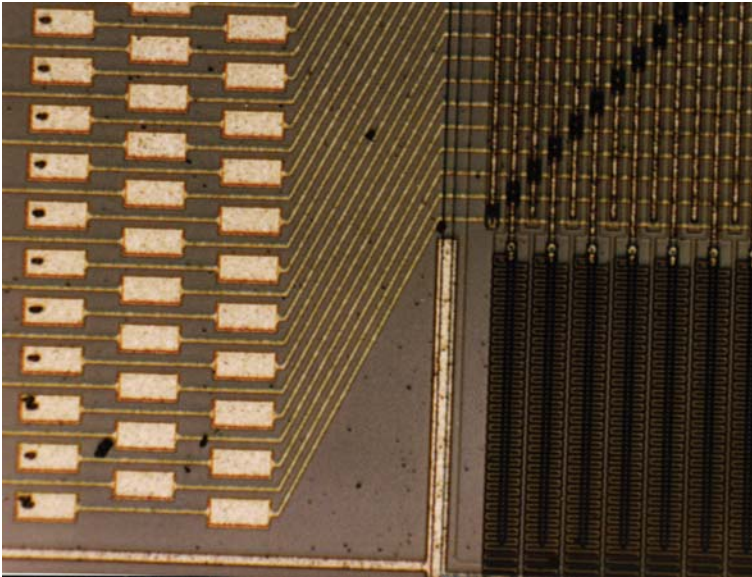


Fig. 4.10 The double-sided double metal layer 90° stereo sensor of the SVX II. The bonding pads are located on the left, they are connected to the Al strips on the double metal and are bonded to the readout electronics. The polysilicon bias resistors are located in the lower right part of the picture, the meander structures. The black spots on the upper right are the vias connecting signal lines to readout lines

technology. A more detailed description of the advantages of 6 in. technology is presented in Sect. 4.3 and in the summary of sensor parameters in Table 4.2.

Intermediate Silicon Layers (ISL)

The intermediate silicon layers 5 and 6, both consisting of double-sided silicon strip detectors, measure both the $R\phi$ and Rz coordinates. The strips on one side of the wafers are parallel to the beam axis (z -axis) while the strips on the other side are tilted by 1.2° . This allows the measurement of the Rz coordinate with low ambiguity⁶ and no additional double metal layer. The ISL layers are mounted at the radii 20 and 28 cm. The overall length of the ISL is 195 cm, covering the pseudo-rapidity region $|\eta| \leq 2$. This special long configuration enables “forward” tracking without forward structures. The whole support structure – the spaceframe – was designed with respect to weight, stiffness and material budget, which led to a carbon-fibre structure. The mechanical arrangement can be seen in Fig. 4.11 and an impressive view is shown in Fig. 4.12, a photo of the ISL before it was closed and inserted into

⁶ The angle of 1.2° allows the connection of strips of several consecutive sensors to one single electronic readout channel, as opposed to layers with a stereo angle of 90° where multiple strips are connected to one routing line, hence to one readout channel.

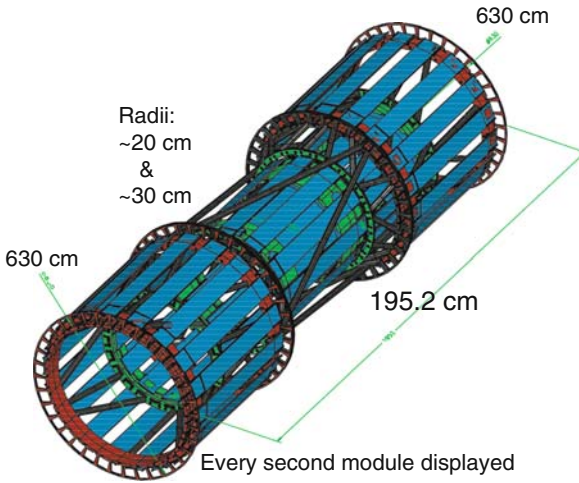


Fig. 4.11 The intermediate silicon layers detector – ISL. The schematic shows the design drawings of the carbon-fibre spaceframe. The geometrical concept of the single additional layer in the central region and the two additional layers in the forward direction can be seen. The carbon-fibre rings are connected with hollow carbon-fibre rods. The total weight of the structure is about 6 kg before mounting the modules [82]

the COT. The early design is described in [148]. Figure 4.13 allows a glimpse into the detector, the space where finally the SVX II was located. In contrast to SVX II, ISL was designed with simplicity in mind. A more detailed description of the ISL can be found in [82, 83]. The ISL sensors are also AC coupled, polysilicon biased and double sided, with $p+$ stop configuration on the n -side. For the larger radii,

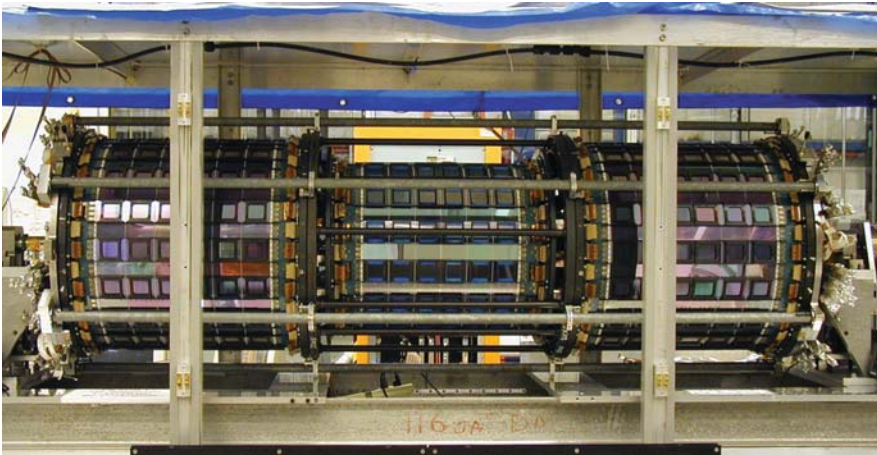


Fig. 4.12 The intermediate silicon layers detector [Courtesy of CDF, Fermilab]

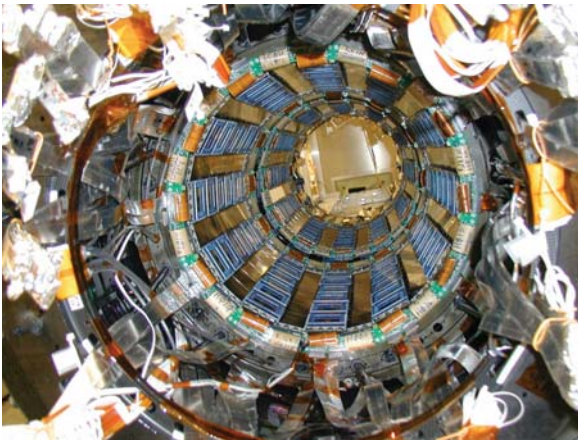


Fig. 4.13 Into the ISL. The full ladders, six sensor long with readout electronics on both sides, are visible in a barrel configuration a rare view during construction [Courtesy of CDF, Fermilab]

occupancy and radiation damage are lower. It is therefore possible to use longer strips and pitches are relaxed to $112\ \mu\text{m}$ on the $R\phi$ and stereo side. This is also necessary to reduce the number of readout channels, thus the costs of front-end electronics and DAQ equipment. Sensors from both old 4 in. and new 6 in. technologies [29, 83] are used. In the 6 in. case, two sensors are processed on a single wafer, see Fig. 4.16. Pitch adapters are used to bring the signals from the strips to the more closely spaced inputs of the SVX3 chips. The ISL ladders are composed of six sensors arranged as half-ladders of three sensors each with a double-sided hybrid at each half-ladder end. A total of 296 half-ladders form 148 full ladders summing up to a total of 888 sensors with 2368 chips. The ladders are composed of carbon fibre. The assembly fixture is displayed in Fig. 4.14. Relaxed space constraints in the high radius regions allow overlapping of ladders even for the z -coordinate.

Central Outer Tracker (COT)

The COT is an open drift chamber with an inner radius of $R = 44\ \text{cm}$ and an outer radius of $R = 132\ \text{cm}$ and a coverage in η up to $|\eta| \leq 1$. It replaces the CTC (Central Tracking Chamber) used in RUN I. Four axial and four stereo “superlayers” provide 96 measurements,⁷ resulting in a total of 2520 drift cells and 30240 readout channels. The different wire angles with respect to Rz in each “superlayer” are $+3^\circ$ $0-3^\circ$ $0+3^\circ$ $0-3^\circ$. The location is shown in Figs. 4.1 and 4.4. The main changes in the upgrade are the small drift cells with a maximum drift distance of $0.88\ \text{cm}$ and fast gas to limit drift times of less than $100\ \text{ns}$. The readout is realized via a pipelined

⁷ One “superlayer” provides 12 measurement points.

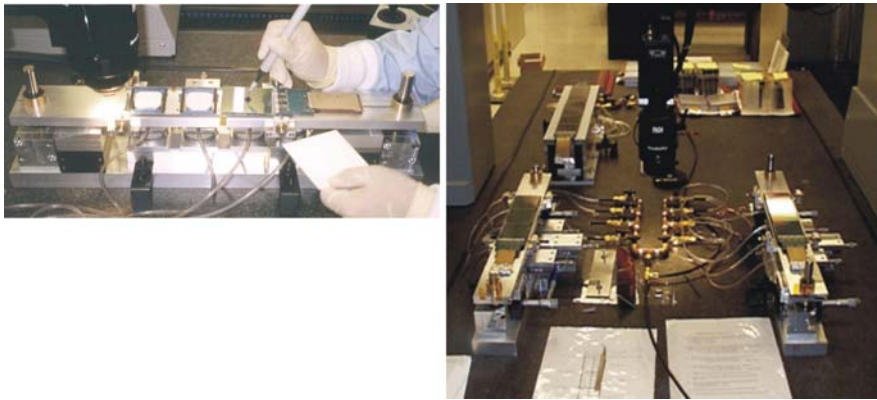


Fig. 4.14 Manual assembly of the CDF ISL ladders. The sensors resting on vacuum chucks were aligned and glued to the supports. The right picture show three half-ladders to complete the curing of the glue

TDC⁸ system. The COT is also equipped with the possibility to measure dE/dx for particle identification. The measurement is complementary to the time-of-flight method. A more detailed description is given in [38].

The SVX3 chip [38, 70, 71]

All silicon sensors are read out by the SVX3 chip, a radiation-tolerant CMOS custom-integrated circuit. Each chip has 128 parallel input channels. The chip consists of two parts built into a monolithic structure: the front-end for the analog functions and the back-end part for the digital functions. The input amplifiers, integrators, the 46 cell pipelines needed for dead-timeless operation and the pipeline acquisition logic is located in the front-end. Up to four groups of cells can be queued for digitization and then read out at one time. The back-end consists of an 8-bit Wilkinson ADC a readout FIFO⁹ and differential output drivers. The chip is able to work with positive and negative signals to handle double-sided silicon detectors. It has a sparsification mode, a calibration input and is capable of pedestal subtraction at the chip level. The chip is programmable to adjust for different TEVATRON running conditions, e.g. bunch spacings (132 and 396 ns). It can handle strip capacitances from 10 to 35 pF. The pipeline depth, threshold level and bandwidth limit are adjustable. The chip has been irradiated with a ^{60}Co source up to 4 Mrad and was evaluated to perform well¹⁰ [70, 71]. The amplification is 15 mV/fC which corresponds

⁸ Time to Digital Converter: **TDC**.

⁹ First In First Out (**FIFO**): Register where the data entered at the input appears in the output in the same order.

¹⁰ During RUN II the chip will be exposed to about 7×10^{13} minimum ionizing particles per cm^2 over a period of 2 years, corresponding to an absorbed dose of 2 Mrad at the inner layer of SVX II [18].

to 60 mV for a minimum ionizing particle. The chip provides dead-timeless readout with level 1 trigger rates up to 50 kHz. The maximum delay between the level 1 trigger decision and read out without overwriting the pipeline cell content is 5.5 μ s at 132 ns between beam crossings.

Silicon Vertex Tracker (SVT) – Secondary Vertexing

The ability to use impact parameter information in the trigger to detect secondary vertices can substantially increase the physics reach of a hadron collider experiment. Background can be quite substantially reduced e.g. for the process $Z \rightarrow b\bar{b}$. The B -decay studies will also be greatly enhanced. Some physics processes not involving b quarks will also profit from the SVT e.g. the high $p_{\perp}$ inclusive muon trigger, needed for the W-mass measurement, has a high level 2 rate. The SVT can both reduce the accidental rate by demanding an SVX II track pointing to the primary vertex and remove lower $p_{\perp}$ muon background by using improved momentum resolution to tighten the $p_{\perp}$ threshold. In order to obtain impact parameter information at level 2 the silicon tracker is read out after each level 1 trigger. The SVT combines data with the level 1 tracking information from the COT and computes track parameters (ϕ , $p_{\perp}$ and impact parameter d_0) with a resolution and efficiency comparable to full offline analysis [38, 124]. The SVT also introduced several hard constraints on the detector design and assembly:

- wedge geometry – compatible with hardware regional track reconstruction
- very tight mechanical tolerances – placement precision of 100 μ m and better with respect to beam
- dead-timeless readout with onboard digitization, sparsification and buffering
- dedicated DAQ pipeline for processing and control only for the SVX

The implementation of a silicon level 2 hardware trigger on impact parameter information is unprecedented in a hadron collider detector.

4.3 Six Inch, a New Technology Step for Large Silicon Applications

The fabrication of microstrip detectors on 4 in. high resistivity wafers allowing a maximum processable area up to 42 cm² has been established at LEP and RUN I at the TEVATRON. The workable area using 6 in. wafers increases up to 100 cm². Figure 4.15 shows a photo of a full wafer.

Since this is twice the area of a 4 in. wafer a larger number of sensors can be processed at the same time on the same wafer resulting in significant reduction of cost. CDF is the first HEP experiment using 6 in. sensors [28, 29, 83]. Figures 4.16 show the mask layout of the 6 in. wafers for ISL and SVX II sensors, respectively. In the case of the ISL wafer both sensors are identical in size. In the SVX II wafer the

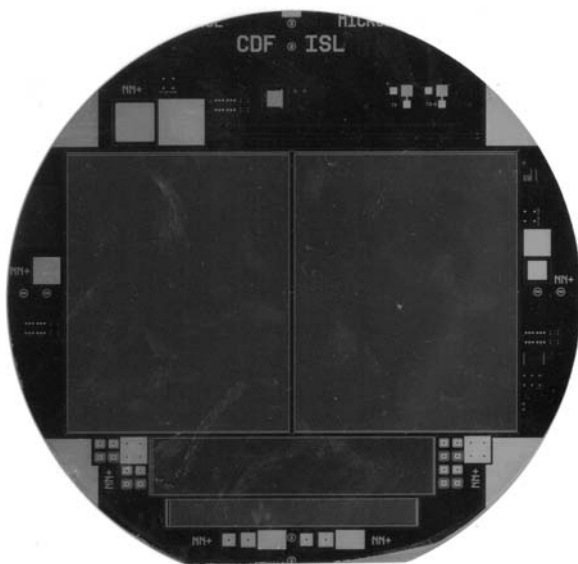


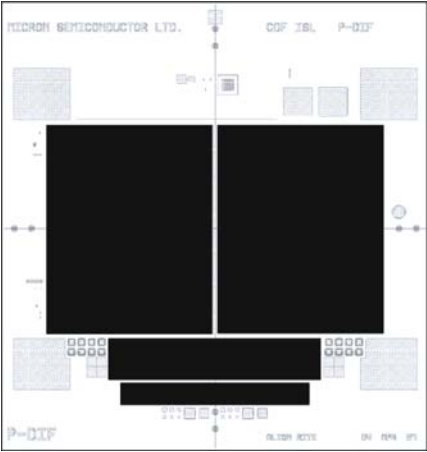
Fig. 4.15 Photo of a full 6 in. ISL wafer – real size*0.5. Two ISL sensors plus two smaller study sensors and many small test structures like diodes and resistors can be seen. The four rounded fully metallized triangles at the perimeter are for handling purposes

sensors are produced for layers at different radii and hence have different geometries, specifically widths. In contrast to the production on 4 in. wafers, the cost of one mask set is saved which is a substantial fraction of the total cost, especially for double-sided sensors and small volume production. The ISL sensors on 6 in. design are even 5.75 mm longer than their counterpart in 4 in. design. Figure 4.17 shows the different electrical structures of an ISL sensor. A photo of the sensor surface (n-side) is shown in Fig. 4.18.

All sensors for SVX II and ISL were AC coupled, polysilicon biased, double sided, produced out of $\langle 100 \rangle$ wafers. For $90^\circ R_z$ readout strips a double metal was implemented over a $5\text{ }\mu\text{m}$ thick isolation to route the strips to the hybrid at the end of the ladders. Large thickness¹¹ of metal-to-metal isolation is mandatory to suppress cross talk and keep capacitance low, especially parasitic capacitance. Also the aluminium trace widths are reduced to $8\text{ }\mu\text{m}$ to reduce capacitance. Two or four sensors were connected to one hybrid for SVX II and ISL, respectively. Coupling capacitor isolation was achieved with a pattern of silicon oxide and silicon nitride. The aluminium strip width was $6\text{ }\mu\text{m}$ smaller than the implant width below to suppress micro-discharge. All corners and edges have a radius of $>10\text{ }\mu\text{m}$ to avoid high fields and any doped region has a concentration of at least 10^{14} ions/cm^2 to ensure radiation hardness. An active $n+$ edge field shaper structure is implemented, refer to

¹¹ Note that the double metal scheme was only applied to 4 in. wafers; for 6 in. wafers mechanical stress imposed by the thick oxide would have violated manufacturer design rules. Sensor bow would have been large, probably large enough to break processed structures.

Mask layout of the 6 in. design



Two sensors fit on one wafer

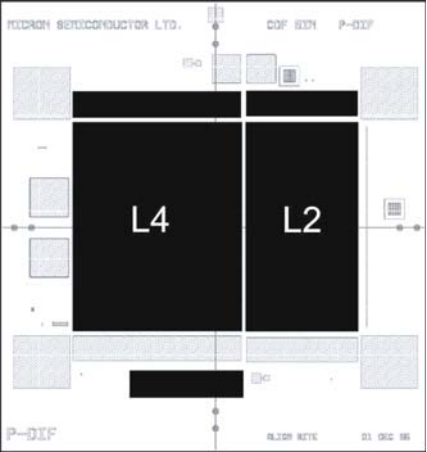


Fig. 4.16 Mask layout of an ISL and a SVX II wafer. Two sensors fit on one wafer. On an ISL wafer is shown with two identical sensors, while on the right the SVX II wafer carries sensors with different layout – a layer 2 (L2) and a layer 4 (L4) sensor. At the bottom, mini sensors and test structures are placed

Layout of the 6 in. design.

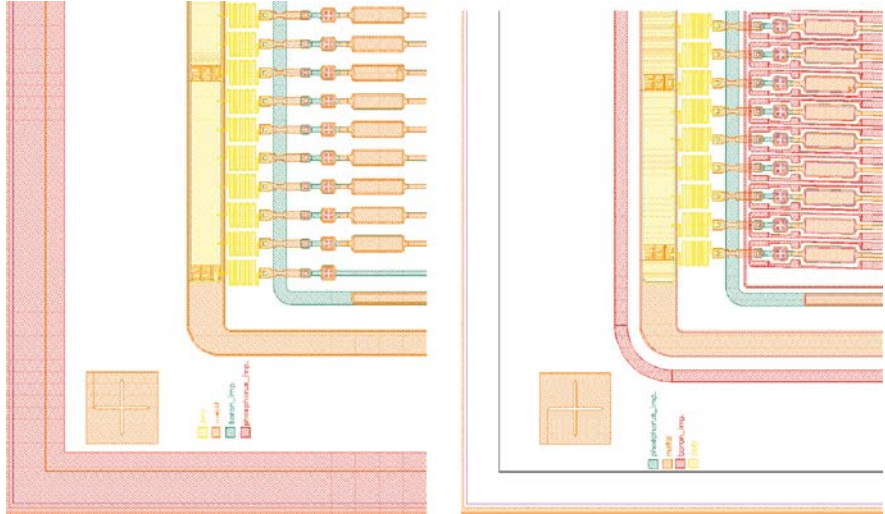


Fig. 4.17 Structure of an ISL sensor – p-side (*left*) and n-side (*right*). All 6 in. sensors for ISL and SVX II are 300 μm thick on $\langle 100 \rangle$ oriented floatzone silicon. The sensors are double sided, single metal, AC coupled, polysilicon biased, with a common p+ stop structure on the ohmic side for SVX II and isolated p+ stops structure for ISL to guarantee inter-strip isolation

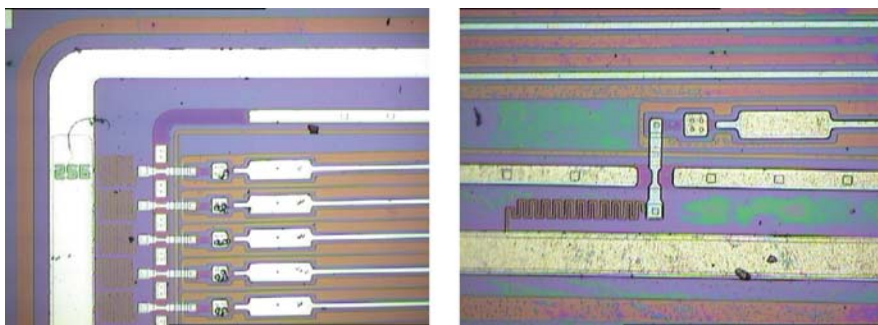


Fig. 4.18 Photo of the stereo n -side of an ISL sensor. The following structures are displayed from left to right, an outer guard ring, the bias ring with meander bias resistors with metal lines passing through the inner main guard ring ending on the small DC pads. The DC pads are then contacting the $p+$ implants by a via. The $n+$ strips are fully surrounded by a $p+$ stop structure. The mentioned inner guard ring is mostly covered by aluminium, the small squares mark the vias. The strips are arranged with a stereo angle of 1.2° with respect to the strips on the junction side.

In the right picture a middle part can be seen where, due to the angle, the strip does not reach the end of the sensor. Therefore the bias resistor angles in from the side

page 34. Strip implants continue below the polysilicon resistors to maximize active surface. More details can also be found in [29, 131].

Initial Problems with First Sensors from 6 in. Wafers

In conclusion switching from 4 to 6 in. sensors was not completely straight forward, it was a bit painful, but feasible. In the end, fabrication on 6 in. sensors is cheaper and performance is as good as for 4 in. Some significant issues related to size increase are shown here, some other problems are presented in Sect. 1.13.

Early Low Capacitances at the Wafer Edges

During the prototype phase, coupling capacitance values decreased significantly towards the wafer edge, dropping below specification limits. The cause was identified to be a non-uniform aluminium sputtering process. The process was not yet fully adapted to larger wafer sizes. This resulted in a substantial over-etching of the Al strips, thereby decreasing aluminium width, thus coupling capacitances. A cartoon of the process problem plus some measurement results are presented in Fig. 4.19.

Two Cases of Low Inter-Strip Resistance

Several sensors were received, showing a defined pattern of several clusters of five consecutive strips with low inter-strip. The problem was tracked down to a

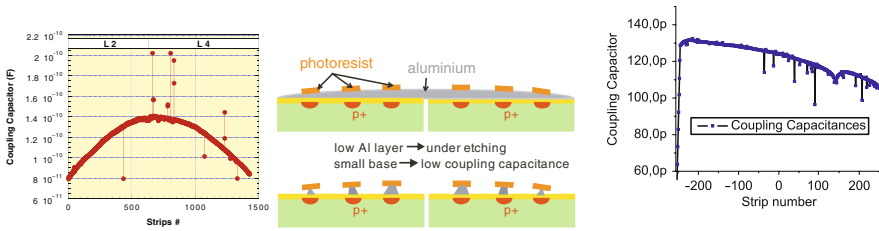


Fig. 4.19 Low coupling capacitances at the edges [29, 83]. On the left a measurement on a full wafer is shown while on the right measurements of an already cut sensor, representing half a wafer is shown. The cartoon in the middle explains how the over-etching happened

PECVD¹² machine. The pattern matches gas outlet positions, where an increased susceptibility to charge-up was introduced. Correct cleaning cured the problem.

A more severe problem is shown in Fig. 4.20 where low inter-strip resistance values were identified on only half of a sensor. The effect was present only on the n -side. Increasing the bias voltage cured the effect completely, leading to the suspicion that the depletion voltage on one half of the sensor is higher, thus the resistivity is lower. This explains why the effect is only present on n -side, because the depletion zone reaches n -side only after full depletion, however CV measurements on diodes

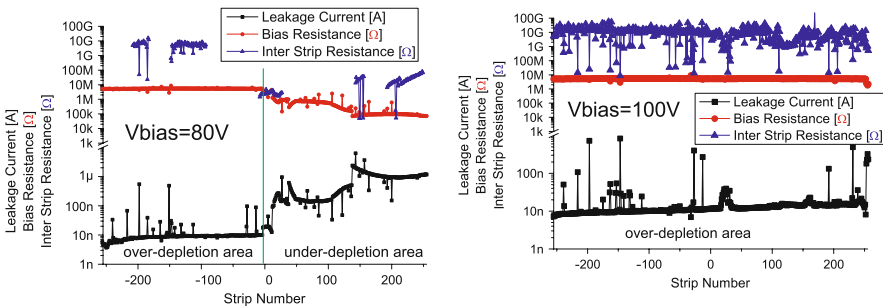


Fig. 4.20 Inter-strip resistance problems due to inhomogeneous wafer material. Half of the sensor shows a low inter-strip resistance on the n -side of the sensor. The effect was identified by leakage current and R_{poly} measurement and confirmed with a full R_{int} measurement. Low R_{int} connects strips, therefore current measurement also collects components from neighbour strips and bias resistors are now arranged in parallel configuration. Different bias voltages were applied during the left ($V_{\text{bias}} = 80 \text{ V}$) and right ($V_{\text{bias}} = 100 \text{ V}$) measurement. While only half of the sensor was full depleted with $V_{\text{bias}} = 80 \text{ V}$, the whole sensor was fully depleted at $V_{\text{bias}} = 100 \text{ V}$. This bias or full depletion characteristic can be explained by a inhomogeneous resistivity of the silicon wafer. Since, in the ISL case, the sensor only covers half of the wafer the decrease of resistivity towards the center of the wafer translates to a decrease in one sensor to one side.

¹² Plasma-enhanced chemical vapour deposition: **PECVD**.

contradicted this hypothesis. It was found later that the 6 in. wafer had a resistivity drop in the centre¹³ of the wafer. A good fraction of sensors had to be rejected.

Another problem with a low inter-strip resistivity encountered during the CDF quality assurance is presented in Sect. 1.13 where the sensor surface was charged up during transport.

All the problems encountered during prototype phase and first production runs were identified and solved.

4.4 Lessons Learned from Operation

In this chapter some incidents that occurred during commissioning and operation will be listed. It is a tale of unexpected incidents to be expected in future experiments. The CDF silicon detector was installed in February 2001. Commissioning of the CDFII silicon detector took place until spring 2002 [30].

Initially, the cooling lines to the central ISL barrel were blocked by remains of epoxy. This blockage was later solved by introducing a boroscope with a surgical laser to bore the glue out.

Failing power supplies and pick-up noise on the layer 00 had to be countered by a special readout arrangement.

A much more severe and unexpected phenomenon was identified when a substantial fraction of modules failed (14/704) long after the commissioning phase. The rate was not compatible with the expected infant mortality rate. The failure was strongly correlated with the trigger frequency. The wire-bonds, perpendicular to the 1.4 T magnetic field carry power for the SVX3D chips from the $R\phi$ to the R_z side of the SVX II hybrids. Any current fluctuations induce a changing Lorentz force on the wires. During consecutive, synchronous chip readout, these forces drive the wires to resonate and cause them to break. A new VME board was introduced to prevent wire-bond resonances by stopping the readout when the trigger rate exceeds a certain frequency. Since installation of the board no further wire-bond failures have been encountered. In addition, the digital current consumption of the SVX3 chips has been lowered by reducing the power output of their digital drivers. Further detailed discussions about this topic can be found in [31].

Another set of very serious incidents were beam incidents from the TEVATRON where the detector was subjected to high dose rates of $\geq 10^7$ MIPs/cm² in a period of time ≤ 150 ns. During the first weeks after an incident the affected readout chips returned data with bit errors. After some months at least some of the affected readout chips recovered. As a consequence a fast interlock, aborting the beam before it has time to de-bunch, has been implemented. In addition, collimators have been installed in order to intercept deflected particles and minimizing the dose rate during an incident. After these implementations no additional damage has been recorded

¹³ With two sensors on one wafer, the effect is present on just half of one sensor.

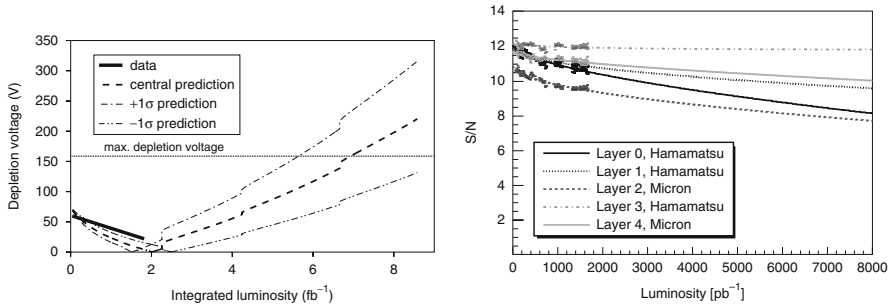


Fig. 4.21 Depletion voltage and signal/noise vs. fluence at CDF. SVX II layer 0 depletion voltage evolution is shown in the left plot. Expectations are met. In the right plot signal/noise values for SVX II together with the predictions are plotted [116]

despite the occurrence of several RF failures and kicker pre-fires. Further details can be found in [30].

A small concern, since non-destructive, is the regular loss of communication to the non-radiation tolerant power supply mainframes in the collision hall. These crates need a reset from time to time, a so-called “hockerization” [87]. During the shutdown 2007/2008 another cooling problem was solved. An acidification of the cooling liquid caused a leak in the cooling joints. In a heroic effort again a boroscope and some catheters plus a small custom-made brass wire were utilized to deposit epoxy from the inside of the tube to the corroded areas [61].

An expected degradation derives from radiation. Signal is constantly decreasing while shot noise is increasing due to the increase of leakage currents. Especially in the inner layers, changes of depletion voltages can be observed. The data follow roughly the expectation given by the Hamburg model. Actually, the effect of radiation damage is being monitored and preliminary results suggest the detector will survive 8 fb^{-1} [61, 116, 159]. Depletion voltage and signal/noise changes vs. fluence is shown in Fig. 4.21. An interesting point in this discussion is the determination of the depletion voltage when a CV scan is not possible. By varying the bias voltage of the silicon sensors, noise values and signal when beam is present are recorded. When the signal maximizes and the noise minimizes or better plateaus their full depletion voltage has been reached. For CDF this is a manual operation and does not work in parallel to data taking.

Today the CDF Run II silicon detector is running with 92% of all sensors and with a data-taking efficiency greater than 97%. Maintaining the detector at a high efficiency level requires a significant effort compared to other CDF sub detector systems, especially in terms of human resources. At least two of about 10 silicon operations group members are on 24-h call.

4.5 The t Discovery, CP Violation in the b Quark Sector

How can precise track and vertex information help to reduce background? An impressive example is given in [117] where the $B^\pm \rightarrow J/\Psi K^\pm$ mass spectra is given with and without SVX $c\tau > 100\mu\text{m}$ cut, see Fig. 4.22. The cuts allow for fully reconstructed exclusive decays of b -hadrons together with a precise hadron momentum measurement in the magnetic field. This capability is also a milestone for any attempt to measure CP violation in the B sector.

In 1994 the evidence of a top quark was published in [3] – a milestone in particle physics finally achieved. Detailed descriptions are written in [4, 75, 88, 154]. Some brief analysis descriptions are presented where the SVX was instrumental in the initial identification. In later stages the SVX II with its larger coverage played also a vital role to reduce background for precision measurements. At the TEVATRON top quarks are produced $\sim 90\%$ of the time by quark–anti-quark ($q\bar{q}$) annihilation into a gluon which then decay into $t\bar{t}$. Within the Standard model, the dominant decay is then

$$t\bar{t} \rightarrow W^+ b, W^- \bar{b} \quad (4.2)$$

with further decay of W

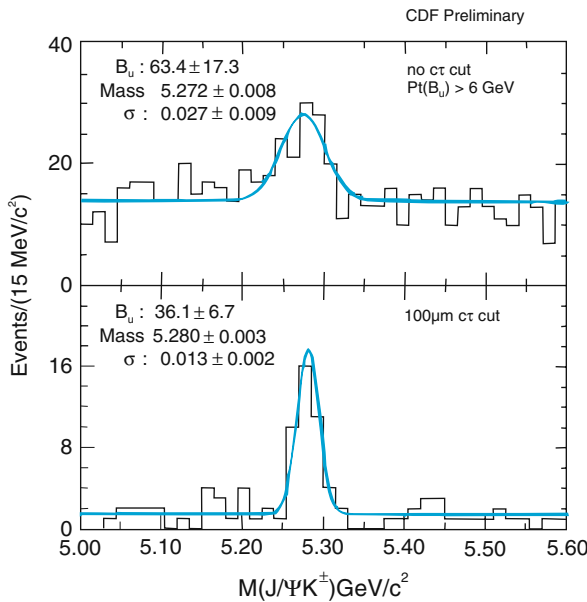


Fig. 4.22 Mass determination without/with vertex cut at CDF [117]. The $c\tau$ cut reduces background drastically thus reducing the statistical error. This is especially important for a hadron collider environment

$$W \rightarrow \begin{cases} (u\bar{d}), (c\bar{s}) & \text{hadronic decay with branching ratio BR : } 2/6 \\ (e\nu, \mu\nu, \tau\nu) & \text{leptonic decay with branching ratio BR : } 1/3 \end{cases} \quad (4.3)$$

The W decay products categorize the $t\bar{t}$ events into “full hadronic”, “di-lepton” or “lepton + jet” channels, but there are always two additional b quark decays which may be “tagged” by a displaced vertex and/or another lepton if the b or a secondary charm decay is semileptonic. In the initial “evidence” paper only “di-lepton” and “lepton + jet + b – tag” channels were analyzed.

The “lepton + jet” channel has a high $p_{\perp}$ lepton, missing energy and two jets from the W decay plus two b jets. Initially, the kinematic cuts, number of jet cuts, plus jet mass cuts did not find enough events to significantly beat the background to claim “evidence”. The identified sample of 52 events can be further constrained by a SVX b -tag down to six events with W plus three or more jet events with a b -tag above 2.3 ± 0.26 expected background events. An alternative b -tagging method

e + 4 jet event

40758_44414
24-September, 1992

TWO jets tagged by SVX

fit top mass is 170 ± 10 GeV

e^+ , Missing E_T , jet #4 from top
jets 1,2,3 from top (2&3 from W)

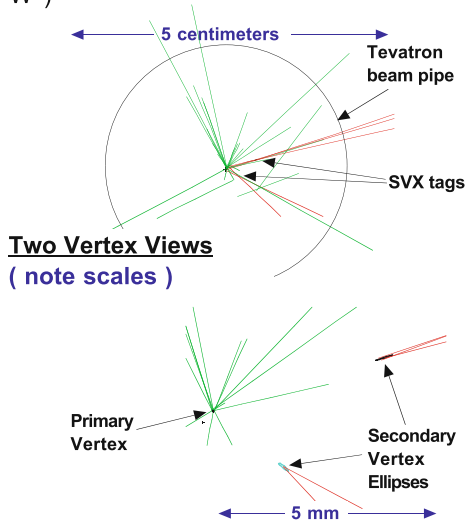
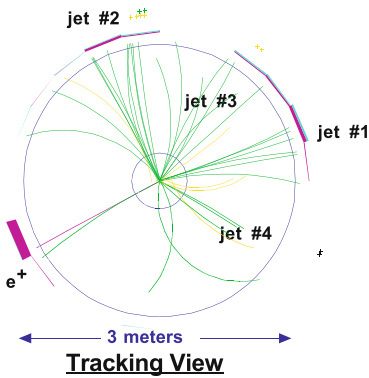
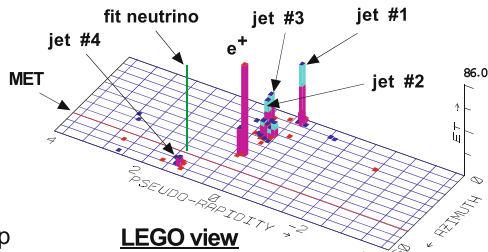


Fig. 4.23 A “Golden” t event. $t\bar{t}$ decaying into W^+b , W^-b , where one W decays leptonically with the signature lepton ID plus missing energy, the second W decays into $q\bar{q}$ resulting in two jets together with the initial two tagged b jets. In total one lepton, four jets, two tagged b jets and missing energy were reconstructed [151]

by identifying “soft” leptons from ($b \rightarrow l\nu_l X$ or $b \rightarrow c \rightarrow l\nu_l X$) with the calorimeter and CTC will not be elaborated here. In summary the “lepton + jet” event type, particularly with a b -tag, is considered the most powerful signature due to a combination of cleanliness and statistics. To improve this method a longer SVX is needed as realized in the RUN II upgrade. An event display is shown in Fig. 4.23 – The Golden TOP event.

Thomas Müller said, when asked about the physics success of the CDF experiment

On a conference in 1983, the theorist John Ellis from CERN instructed us experimental particle physicists to find ways for identifying experimentally beauty quarks in particle jets. Ten years later, first evidence for top quark signals was obtained in the CDF experiment using the reconstruction of beauty hadron decays. Any claims for the observation of top quarks would have been very doubtful without the excellent performance of the silicon vertex detector.

There are many more exciting physics subjects like CP violation in the B sector to determine the CP violating phase β_s or B_s^0 – $\bar{B}_s^0$ oscillations [6, 145]. Spectroscopy (mass, lifetime, decays) of $B_c, B_s, \Lambda_b, \Xi_b, \Sigma_b$, orbitally excited B -mesons, etc. The SVT enhanced especially the B spectroscopy. It highly enriched the statistical sample on hadronic B -decays, which have an intrinsic good $p_\perp$ resolution (no neutrino). The SVT was the key for the B_s measurement. The field is rich. First observation of charged Σ_b and first direct observation of Ξ_b at the TEVATRON plus some more examples are discussed in [135].

Additionally, for some topics a simple b flightpath tag is not enough, e.g. for all the CP and oscillation studies. The correct flavour must be known. To “tag” the true flavour of the B -meson the charge must be known. Two methods were developed: (1) The “opposite side tagging” where the jet charge or the lepton charge ($b \rightarrow l^-$ but $\bar{b} \rightarrow l^+$) is evaluated on the “other” B -hadron to determine the B -hadron flavour of interest. (2) The “same side tagging” method where the charges of the particle of associated production are determined, e.g. $\pi^+(\pi^-)$ is associated with the formation of a B ($\bar{B}$) meson. The mechanisms were developed during RUN I and perfected in RUN II. As mentioned earlier, the purpose of vertex detectors is simply to measure precise tracks and tag the flavour of heavy quarks.

Chapter 5

CMS: Increasing Size by 2 Orders of Magnitude

The Compact Muon Solenoid (CMS) operates at the *Large Hadron Collider* (LHC) at CERN. It was conceived to study proton–proton (and nucleon–nucleon) collisions at a center-of-mass energy of 14 TeV (5.5 TeV) and at luminosities up to $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ ($10^{27} \text{ cm}^{-2} \text{ s}^{-1}$). The detector is characterized by high hermeticity and compactness. A 3.8 T superconducting solenoid surrounds a silicon tracker, an electromagnetic *calorimeter* (ECAL) and a *hadron calorimeter* (HCAL). The return yoke is instrumented with muon detectors covering most of the 4π solid angle. Forward sampling calorimeters extend the CMS pseudo-rapidity coverage at high $|\eta|$ values. The detector is fully described in [2, 40–42]. Its layout can be seen in Fig. 5.1. The CMS detector was fully constructed on the surface and was lowered 100 m down to the cavern in 11 slices. Individual slices weighted up to 2500 t summing up to a weight of 12500 t. The inner detectors like calorimeters and tracking detectors were inserted and instrumented later down in the cavern. In the following the CMS silicon tracker will be described.

December 1999, on the eve of the last millennium, the CMS Tracker Collaboration decided to construct its tracker fully out of silicon, summing up to 206 m^2 silicon surface.¹ The design goal of the tracker is to operate with a maximum of 1% occupancy at all layers and a good impact parameter resolution in $R\phi$ and R_z . The requirements are

- efficient and robust pattern recognition
- fine granularity to resolve nearby tracks
- fast response time to resolve bunch crossings
- ability to reconstruct heavy objects translating to 1–2% $p_{\perp}$ resolution at $\sim 100 \text{ GeV}$
- ability to operate in a crowded environment at 10 cm from primary vertex
- ability to tag b/τ through secondary vertices
- reconstruction efficiency: 95% for hadronic isolated high $p_{\perp}$ tracks and 90% for high $p_{\perp}$ tracks inside jets
- ability to operate in a very high radiation environment
- efficient and precise tracking in the pseudo-rapidity range $|\eta| \leq 2.5$.

¹ Prior to this meeting about 70 m^2 silicon plus $\sim 200 \text{ m}^2$ microstrip gas counters (MSGC) were specified in the initial TDR.

CMS layout and detectors

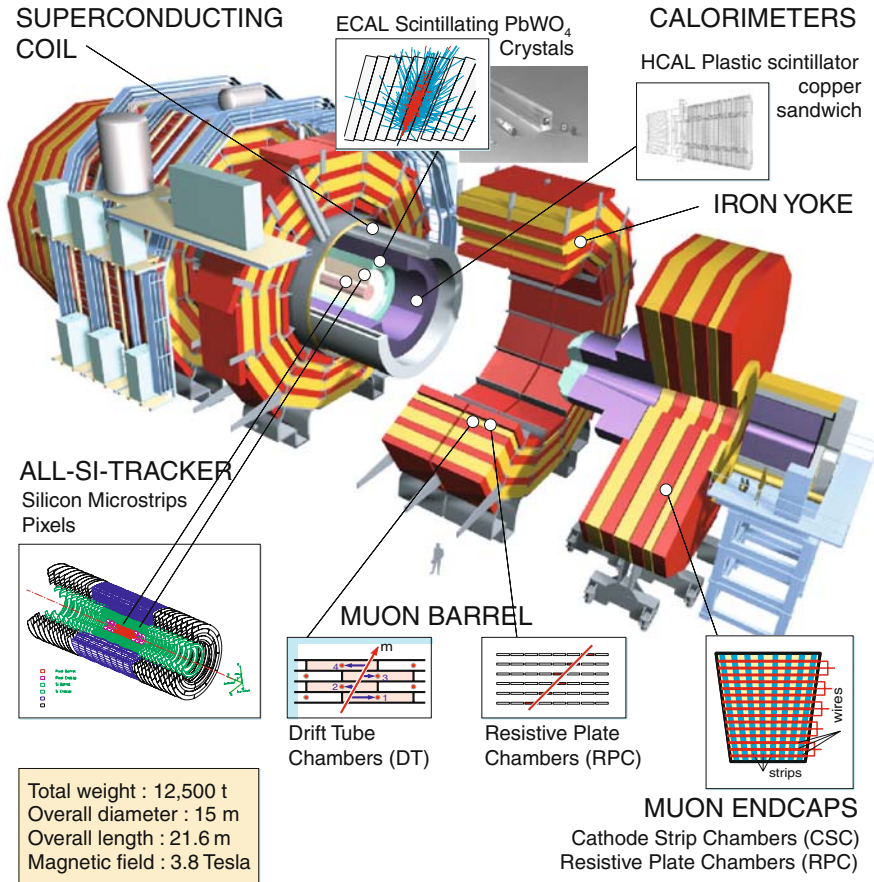


Fig. 5.1 The CMS detector and its components [Courtesy of CERN, 152]

The result is a small pixelated detector in the centre with a large volume strip detector surrounding it. All in all a cylinder of 2.5 m diameter and 5.4 m length is instrumented with 206 m² of active silicon detectors. The general 3D layout can be seen in Fig. 5.2. At the design luminosity of $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ the tracker will see around 1000 particles from about 20 overlapping proton–proton collisions per bunch crossing, every 25 ns. With a homogeneous field of 3.8 T, low momentum particles spiral at low radii and therefore the occupancy decreases faster than $1/r^2$ as it would without a magnetic field. Fast readout and high granularity are needed to achieve the low design occupancy, get a reasonable track separation and good impact parameter resolution σd_0 .

The CMS tracker is composed of a pixel detector with 3 barrel layers and a silicon strip tracker with 10 barrel detection layers extending outwards to a radius of 1.1 m.

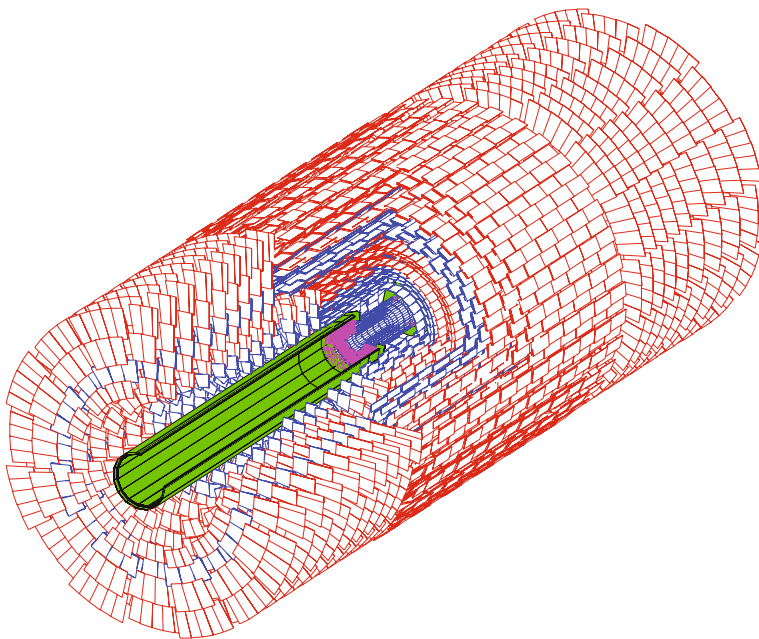


Fig. 5.2 The CMS all-silicon tracker layout [79]. The pixel detector is located in the center. It is surrounded by 10 strip barrel layers supplemented by 3 small forward and 9 large forward disks. The barrel layer 1,2,5,6 and endcap rings 1,2,5 consist of double modules, mounted back to back with a stereo angle of 100 mrad. The overall length and diameter is 5.4 and 2.4 m, respectively. About 1440 pixel and 15148 strip detector modules build up the tracker. All in all 66 million pixel cells and 10 million strips are available. The tracker directly surrounds the beam pipe and is enclosed by the electromagnetic calorimeter; no additional inner tracking device like a drift chamber or transition radiation tracker is installed [84]

Each system is completed by endcaps which consist of two pixel disks in the pixel detector and three small plus nine large disks in the strip tracker on each side of the barrel extending the acceptance of the tracker up to a pseudo-rapidity of $|\eta| < 2.5$.

The CMS Pixel Detector

In order to keep the occupancy at or below 1% pixelated detectors have to be used at radii below 10 cm. For a pixel size of $100 \times 150 \mu\text{m}^2$ in $R\phi$ and Rz , respectively, which is driven by the desired impact parameter resolution, the occupancy is of the order 10^{-4} per pixel at LHC bunch crossing. With analog signal interpolation, a hit resolution of $10(R\phi) \times 20 \mu\text{m}(Rz)$ can be achieved. Three pixel barrel layers are located at radii 4.4, 7.3 and 10.2 cm. The pixel barrel is 53 cm long. Two pixel forward disks at $z = \pm 34.5$ and $z = \pm 46.5$ cm guarantee the 3D space points coverage up to $|\eta| < 2.5$. With a total area larger than 1 m^2 the CMS pixel detector is as large as the complete DELPHI silicon vertex detector. The pixel detector is displayed in Fig. 5.3.

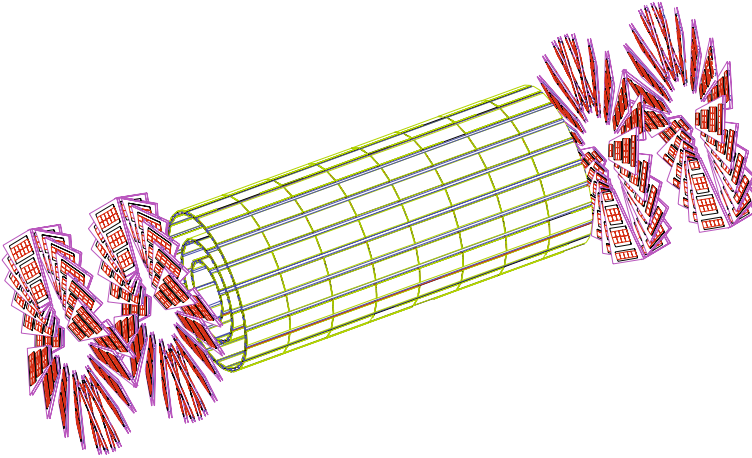


Fig. 5.3 The CMS pixel detector layout. Three 53 cm long barrel layers at radii 4.4, 7.3 and 10.2 cm plus two forward disks at $z = \pm 34.5$ and $z = \pm 46.5$ cm guarantee the 3D space points coverage up to $|\eta| < 2.5$. The barrel (*forward*) pixel detector contains 768 (672) pixel modules with 48 million (18 million) pixel cells covering 0.78 (0.28) m² [60]

The detector is instrumented with 768 pixel modules in the barrel plus 672 modules in the forward disks for a grand total of 66 million pixels. A pixel module including an assembly picture is shown in Fig. 5.4. The pixel detector is essential for b and τ tagging, primary vertex reconstruction. It also determines the track seed towards the outer strip tracker.

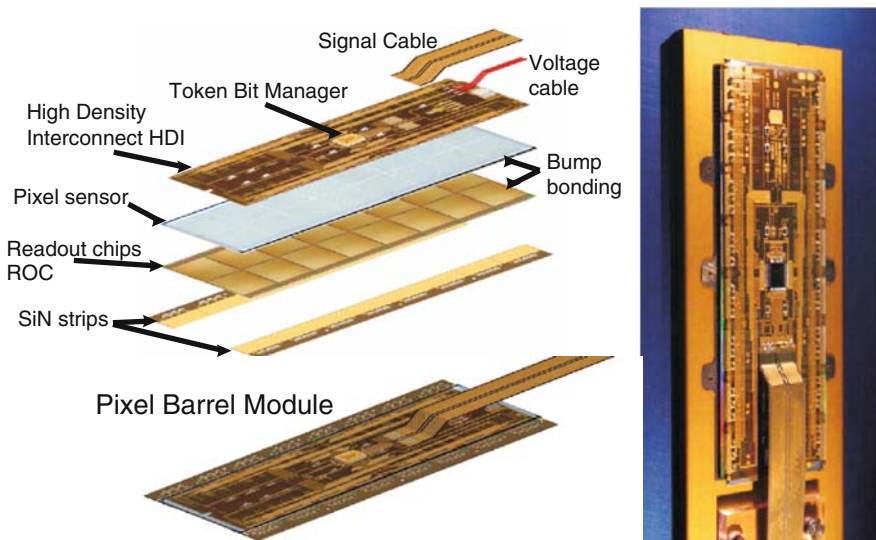


Fig. 5.4 Pixel module – barrel type [44]

Silicon Strip Tracker (SST)

The CMS Silicon Strip Tracker (SST) spanning radii $20\text{ cm} < r < 110\text{ cm}$ plus a substantial forward region is subdivided into *Tracker Inner Barrel* (TIB), *Tracker Inner Disk* (TID), *Tracker Outer Barrel* (TOB) and *Tracker Endcap* (TEC). The sub detectors designs are different to match the requirements at the different radii – a bit like the manifold solutions as for DELPHI and CDF II. The different sub detector locations can be seen in Fig. 5.5, where a quarter section of the detector is presented.

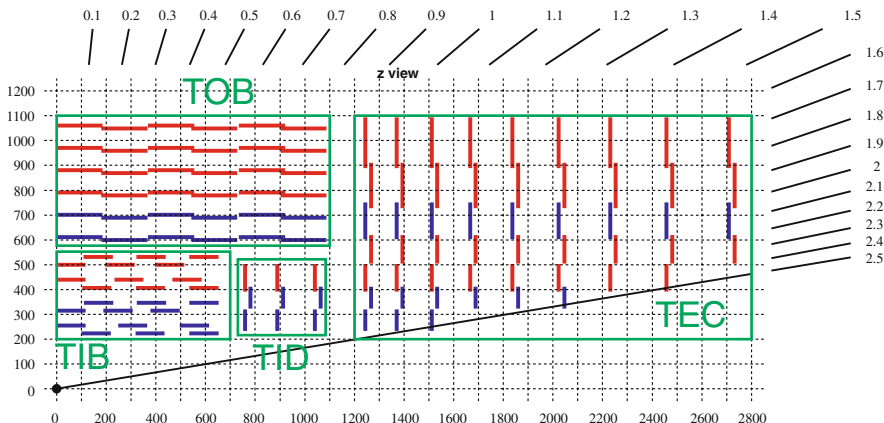


Fig. 5.5 The CMS strip tracker layout. At intermediate radii ($20\text{ cm} < r < 55\text{ cm}$) the reduced particle flux allows the use of silicon microstrip detectors with a typical cell size of $10\text{ cm} \times 80\mu\text{m}$, resulting in an occupancy of up to 2–3% per strip at LHC bunch crossing. In the outer region ($55\text{ cm} < r < 110\text{ cm}$) the strip pitch and length can be further increased to have cell size $20\text{ cm} \times 180\mu\text{m}$. The detector is consequently instrumented with barrel geometry (TIB and TOB) including some stereo modules, complemented with the forward inner disks (TID) and the large endcaps on both sides (TEC). Barrel layer 1, 2, 5, 6, TID ring 1, 2 and TEC ring 1, 2 and 5 are instrumented with stereo double-sided modules

Tracker Inner Barrel (TIB)

The TIB has four barrel layers assembled in shells, layers 1 and 2 are double sided (DS). The TIB is complemented by two disk-shaped forward detectors (TID) each composed of three small disks. The TIB/TID spans the radii $20\text{ cm} < r < 55\text{ cm}$ with a length of 2.2 m ($z < |110\text{ cm}|$). The TIB alone is 1.4 m long ($z < |65\text{ cm}|$). All modules are mounted on “strings” which are directly and individually placed on the structures. The reduced particle flux density allows the use of strip sensors with a typical cell size of $10\text{ cm} \times 80\mu\text{m}$ and $10\text{ cm} \times 120\mu\text{m}$ resulting in an occupancy of up to 2–3% per strip at LHC bunch crossing. Modules are limited to one single sensor to accommodate for the maximum strip length. A photo of the inside of TIB can be found in Fig. 5.6 and a picture of a TID part in Fig. 5.7.

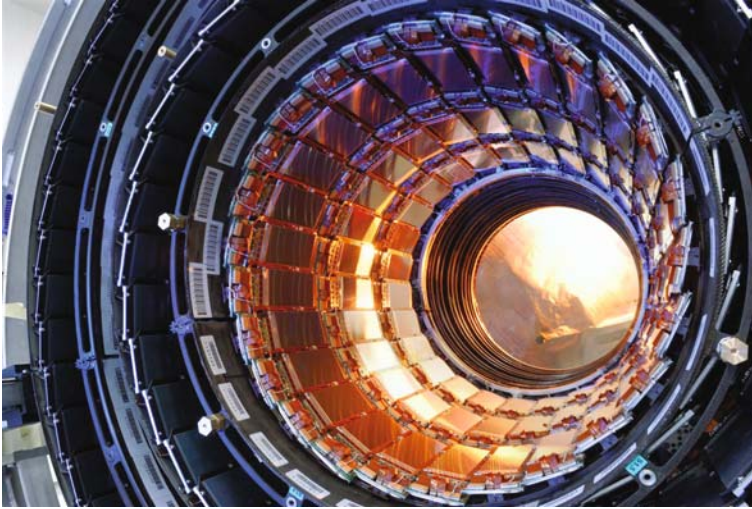
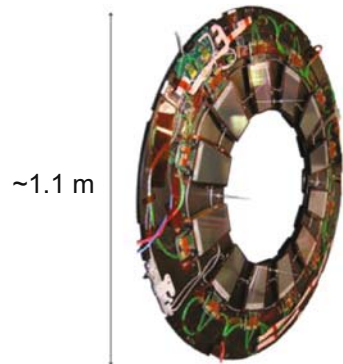


Fig. 5.6 Tracker Inner Barrel (TIB). Three layers of tracker inner barrel detector are visible. In Fig. 5.9 it is inserted into the TOB. Finally, it will house the pixel detector. In the background the inner edges of the three Tracker Inner Discs can be seen [Courtesy of CERN]

Fig. 5.7 One disk of the Tracker Inner Disk (TID). Three of these disks on both TIB sides complete the inner detector fully embedded in the TOB [141]



Tracker Outer Barrel (TOB)

The TOB structure where the modules are assembled in six concentric layers (layers 5 and 6 are DS) surrounds the TIB. It is located inside the electromagnetic calorimeter. The TOB spans radii $55\text{ cm} < r < 110\text{ cm}$ and a length of 2.2 m ($z < |110\text{ cm}|$). For a detector of the size of the TOB an individual module placement is not practical anymore. A structure was designed where 688 one metre long “rods” equipped with modules are inserted. At these radii the pitches and strip lengths can be increased, which helps to moderate the number of readout channels, given the large area. The cell size is $20\text{ cm} \times 120\mu\text{m}$ and $20\text{ cm} \times 180\mu\text{m}$ with two sensors daisy chained to one readout hybrid. The daisy chaining has obvious advantages but also increases

the channel capacitance load, thus the noise. This is compensated by increasing the thickness from $320\text{ }\mu\text{m}$ (“thin”) for TIB/TID to $500\text{ }\mu\text{m}$ (“thick”) for TOB sensors. The same argument and design holds for TEC where inner rings 1–4 are “thin” and ring 5–7 sensors are “thick”. An important detail is the smaller pitch in the two outermost layers reflecting the need to have a precision space point at a large lever arm (Fig. 4.3 on page 127) and a precision link point to the calorimeters. For TIB and TOB, having a barrel-like structure, sensors are rectangular and strips run parallel to the beam (z -axis). A double-sided module is composed out of two single-sided sensors mounted back to back where one is tilted by an angle of 100 mrad with respect to the z -axis. A photo of the TOB and a rod can be seen in Fig. 5.8. Figure 5.9 displays how the TIB is embedded in the TOB.

Tracker End Cap (TEC)

Two tracker endcaps (TEC) ensure a pseudo-rapidity coverage of $\eta \leq 2.5$. The strip orientation is radial, to achieve a continuity of all strips running radially through all rings from ring 1 to ring 7 sensors at different radii. Seven different types are necessary. All sensors are wedge type and outer pitches of e.g. sensor W5A must match inner strip pitches of sensor W5B for all individual strips, refer to Table 5.1.

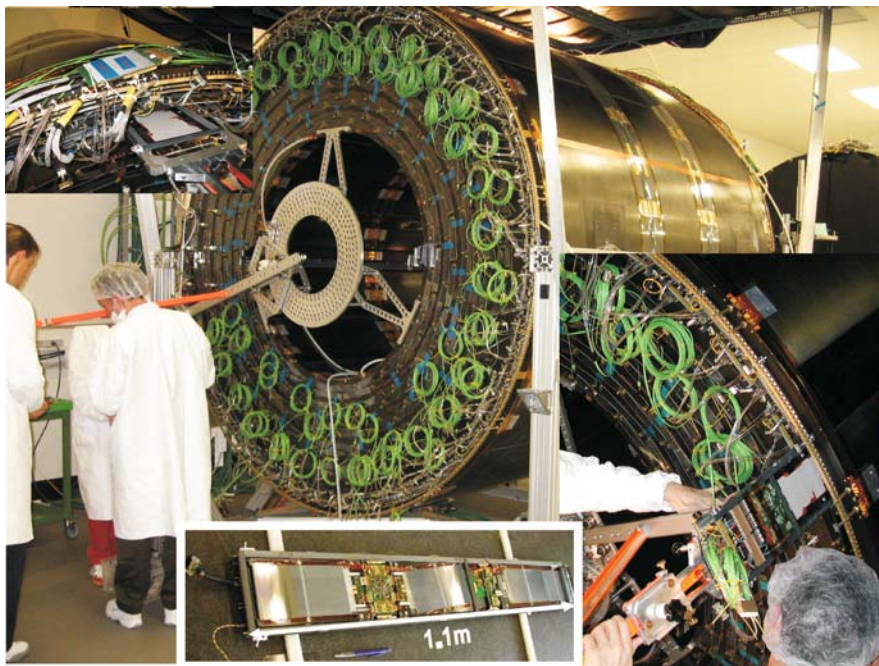


Fig. 5.8 Rod insertion into TOB. The main picture gives a good overview of the size and complexity of the TOB. A special tool guarantees a safe insertion. A rod is displayed at the bottom [84]



Fig. 5.9 TIB inserted in TOB, a rare view. The four layers of the tracker inner barrel are visible inside the tracker outer barrel. The TOB layers 5–10 are completely hidden by the necessary cabling. This is a rare view during the time of construction

Table 5.1 The different sensor types

Sensor type	@ Layer	Trapezoidal a b h [cm]	Stereo module	Pitch [μ m]	No. of strips	Thick [μ m]	Resistivity [k Ω cm]	Sensors module
IB1	1, 2	63.4 63.4 119.2	YES	80	768	320	1.5–3	1
IB2	3, 4	63.4 63.4 119.2		120	512	320	1.5–3	1
OB1	9, 10	96.4 96.4 94.5	L5,L6	122	768	500	3.57.5	2
OB2	5, 6, 7, 8	96.4 96.4 94.5		183	512	500	3.57.5	2
W1TID		63.6 93.8 112.9		80–119	768	320	1.4 –3	1
W1		64.1 88.1 89.5	YES	81–112	768	320	1.5–3	1
W2		88.2 112.4 90.3	YES	113–143	768	320	1.5–3	1
W3		65.0 83.2 112.8		124–158	512	320	1.5–3	1
W4		59.9 73.4 117.4		113–139	512	320	1.5–3	1
W5A		99.0 112.4 84.0	YES	126–143	768	500	3.57.5	+W5B
W5B		112.4 123.0 66.1	YES	143–156	768	500	3.57.5	+W5A
W6A		86.1 97.5 99.0		163–185	512	500	3.57.5	+W6B
W6B		97.5 107.6 87.8		186–205	512	500	3.57.5	+W6A
W7A		74.1 82.9 109.8		140–156	512	500	3.57.5	+W7B
W7B		82.9 90.0 98.8		157–172	512	500	3.57.5	+W7A

The IB stands for inner barrel, the OB for outer barrel and the W for wedge, the sensors in the endcap. a, b defines the width and h the height of the sensors. Note that the OB1 sensors with the narrower pitch are located in the outermost layers to have a precise measurement with a long lever arm. All OB and W5–W7 sensors are 500 μ m thick while all IB and W1–W4 are 320 μ m thick.

The detectors of ring 1, 2, 5 are made of double-sided modules. Modules of ring 1–4 contain a single sensor while ring 5–7 have a larger pitch and two sensors are daisy chained together. As for the TOB the modules are arranged on substructures – on wedge-shaped “petals”. Petals hold up to 7 rings of modules with the different geometries. One TEC consists of 9 disks populated with petals, each covering $1/16$ of 2π . There are eight different petal types varying in radial length, hence number of populated rings, to adapt for the location in z . Petal types differ for disks 1 and 2, 3–6, 7 and 8 and 9, the arrangement can be seen in Fig. 5.5. A total of 288 petals form both endcaps. The detector spans $120\text{ cm} < |z| < 280\text{ cm}$ and $20\text{ cm} < r < 110\text{ cm}$. An impressive photo of the TEC can be seen in Fig. 5.10.

Detailed descriptions of the SST are also to be found in [42, 44, 79, 84]. Table 5.1 informs about all important sensor geometry parameters.

Appreciation of the full CMS detector size and the relation to the tracker can be gained by looking on Fig. 5.11 where the tracker is on the way to its final position in the heart of CMS – December 2007.

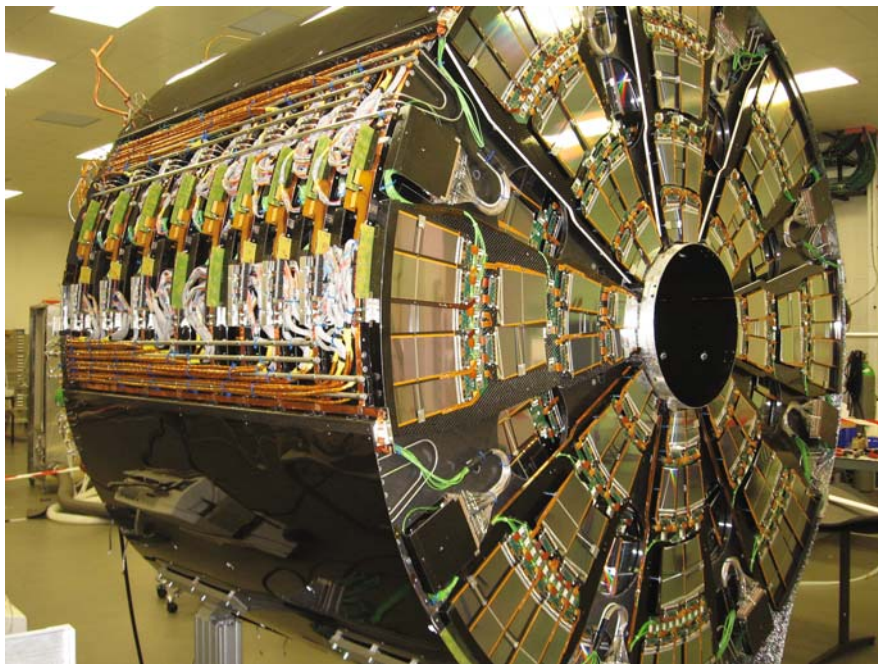


Fig. 5.10 The tracker endcap (TEC), fully equipped and open, a rare view. Eight petals are visible on the front, the space in between is covered with petals on the other non-visible side of the disk. Nine similar disks form one tracker endcap. The 96 visible wedge-shaped sensor modules placed in a wedge geometry on the petals guarantee a continuous-radial strip orientation. On the left an opening shows all the services for one sector, out of eight. The diameter of one TEC is 2.5 m while the length stretches to 1.7 m. One TEC holds 144 petals. All electrical and optical cables and cooling pipes were installed in autumn 2005. Both TECs were fully ready, with all petals installed and inserted into the tracker support tube early 2007

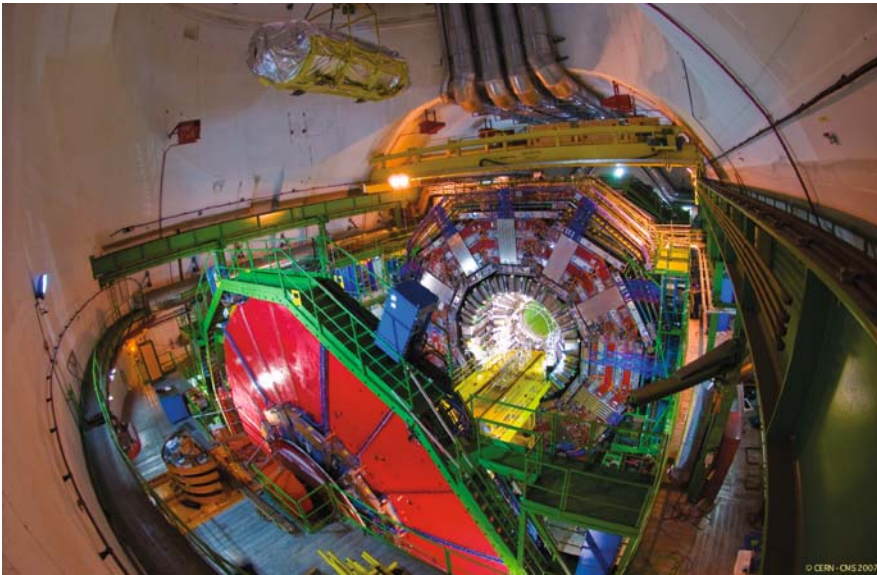


Fig. 5.11 The CMS tracker on its way to the heart of CMS – 2000 man years on a hook. In December 2007 the CMS tracker finally descended down the 100 m deep shaft to be inserted into the heart of the CMS experiment to measure the particle tracks at between 15 and 22 positions in the detector with a precision of better than $20\ \mu\text{m}$. [Courtesy of CERN]

As a result from all necessary services, like cables, cooling pipes, support structures and electronic boards, the material budget is much higher than optimal and it is one of the issues which needs to be improved for any future detector. Figure 5.12 shows the material budget of the CMS tracker in units of radiation length. It increases from $0.3\ X_0$ at $\eta \approx 0$ to about $1.7\ X_0$ at $|\eta| \approx 1.4$, beyond which it falls to about $1\ X_0$ at $|\eta| \approx 2.5$. It is quite obvious that cables and support structures carry most of the weight, also the interface region between sub detectors, between barrel and forward region are prominently too massive.

Nevertheless, the designs described above lead to excellent performance underlined here with the track resolution plots for single traversing muon tracks in Fig. 5.13.

The issues of radiation and appropriate designs are discussed in the next sections. The front-end chip technology choice is presented in Sect. 5.1.1. The sensor design and strategies to achieve the necessary radiation tolerances are expressed in Sect. 5.1.2.

Different from CDF II the CMS tracker is not participating in the hardware-level trigger but tracking information plays a major role in the *high-level* software trigger (HLT) (computer farm). The level 1 hardware trigger reduces the 40 MHz event rate to 100 kHz. The HLT further reduces the data rate to 100 Hz to be stored – refer to Sect. 5.3 later.

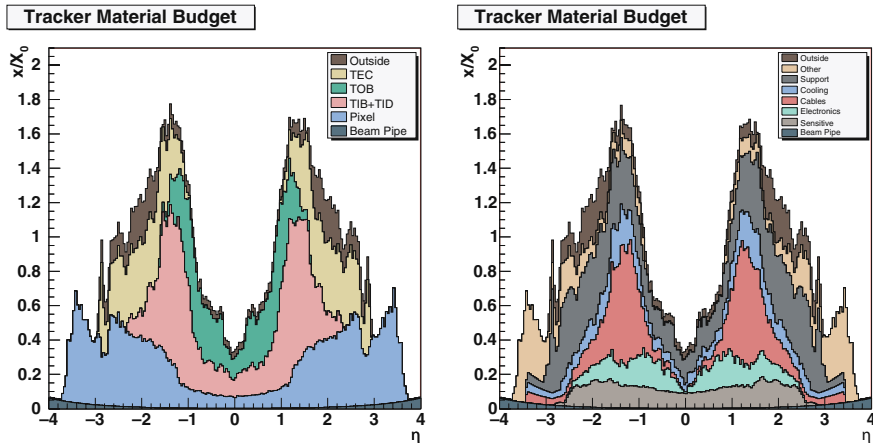


Fig. 5.12 Material budget is displayed in units of radiation length as a function of pseudo-rapidity η for the different sub detectors (*left*) and broken down into the functional contributions (*right*). [42]. A lot of design effort was spent to achieve a “light” tracker, Kapton cables were introduced directly on the flex hybrid with no extra connector; thin-walled cooling pipes were used; low mass power cables (aluminium) run inside the active CMS tracker volume, while outside low resistivity copper cables are used; structural elements are made of light weight carbon fibre and honeycomb structures. The beam pipe is made of beryllium. But despite all these efforts, at the interface of TIB and TOB to TEC all inner cables and pipes have to pass resulting in the two “too” high material peaks at both detector ends at $|\eta| = 1.4$

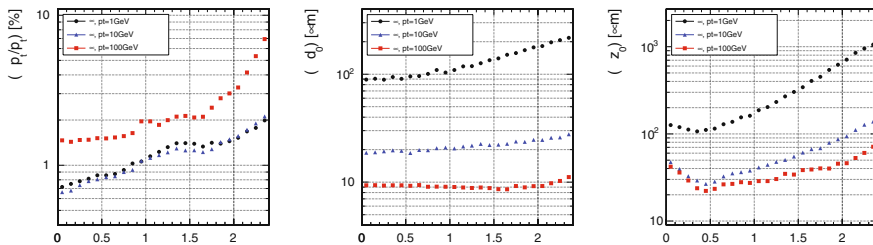


Fig. 5.13 Resolution of several track parameters for single muons with transverse momenta of 1, 10 and 100 GeV: transverse momentum (*left*), transverse impact parameter (middle) and longitudinal impact parameter (*right*) – simulation [42]

5.1 Design, How to Survive 10 Years in the Radiation Environment of LHC

The radiation environment at luminosities of $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ can be translated to integrated fluences² on the order of $\Phi_{eq} = 10^{13} n_{1 \text{ MeV}} / \text{cm}^2$ in the outer strip tracker, $\Phi_{eq} = 1 \cdot 10^{14} n_{1 \text{ MeV}} / \text{cm}^2$ in the inner strip tracker volume for the full

² Reminder: fluence numbers are always given in 1 MeV neutron equivalent/cm² [Φ_{eq}] = $n_{1 \text{ MeV}} / \text{cm}^2$.

operation period of 10 years. The pixel detectors expect to be subjected to even $\Phi_{eq} = 3 \cdot 10^{14} n_1 \text{ MeV/cm}^2$ per year. These numbers are derived from simulations. Detailed numbers per volume cell including the real charge particle/neutron ratio are calculated. This radiation affects the gates in the ASIC transistors as well as the crystal lattice of the sensors. Early ASIC chips of the LEP era or current CDF chips would not survive in the LHC environment. The basics of bulk and surface radiation-induced damages are discussed in Sect. 1.10. In the next sections the dedicated survival strategies of the CMS tracker are discussed.

5.1.1 Electronics – Quarter Micron Technology

In the late 1990s radiation studies on chips proved that the thinner the gate oxides the more radiation tolerant the transistor, thus the electronic device. This was already seen for the different chip versions of LEP and CDF where the decrease in feature size exhibited an increased radiation tolerance with respect to ionizing radiation levels. Within a “thin” oxide there is simply not enough lattice space for an effective defect concentration of holes to form and accumulate. In addition, the probability of electrons “tunnelling” into the oxide from the silicon bulk beneath is higher for a thinner oxide layer. These electrons can then recombine with the trapped holes near the interface. The detailed effect and technology exploitation is described in [94, 95]. The technology is also called “deep sub-micron” or “quarter micron³” and is much more radiation tolerant than any former chip generation.⁴ Unfortunately the use of standard ASIC design libraries from the manufacturer is not sufficient to achieve the necessary radiation tolerance. The feature size defines the gate oxide thickness but there are always neighbouring oxides where surface damage can form and the resulting increasing surface leakage current again renders the transistors useless. The missing link is the full enclosure of all $n+$ diffusions at different potentials including n -wells – fully enclosed NMOS transistors. A schematic is shown in Fig. 5.14. For CMS any larger feature size than 250 nm would not have been radiation tolerant enough. Hybrids equipped with CMS readout chip APV25⁵ were irradiated to fluences of more than 30 years of LHC equivalent and exhibit no degradation.

Gigi Rolandi, the CMS Tracker Project Manager said,

The Quarter Micron technology arrived just in time, without it the realization of our plans would not have been possible!

Both, the pixel readout chip (ROC) and the strip detector chip (APV25) are produced in quarter micron technology.

³ At a feature size of 0.25 μm and below, chips start to be enough radiation tolerant for LHC operation.

⁴ Another radiation-tolerant technology called DMILL existed but there were some production yield problems.

⁵ 0.25 μm version of the APV chip – final version.

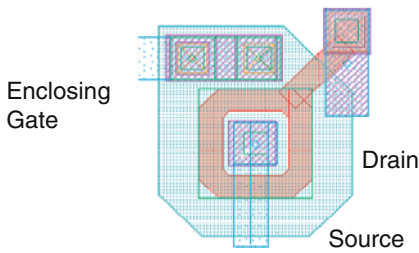


Fig. 5.14 Radiation-tolerant transistor, 0.25 μm , enclosed layout. The gate encloses all n+ regions completely avoiding any thick transistor-relevant oxide structures. This method prevents any radiation surface damage in parasitic thicker side oxides. The thin formed gate oxide is intrinsically radiation tolerant

In a high radiation environment there is also a chance of a state change in the chip microprocessor, the memory cells or the transistors caused by an ionizing particle. These single event upsets have only minor effects in the LHC and are beyond the scope of this book. They were investigated thoroughly and are considered “soft”, while their effects are of a temporary nature. They do not permanently degrade the functionality of chips.

5.1.2 Silicon Sensors

The pixel detector, being subjected to fluences up to $\Phi_{eq} = 3 \cdot 10^{14} n_1 \text{ MeV}/\text{cm}^2$ per year⁶ at nominal LHC luminosity, utilizes different sensor designs and technologies than the strip detector, facing “only” a fluence of $\Phi_{eq} = 1 \cdot 10^{14} n_1 \text{ MeV}/\text{cm}^2$ for the full 10 years of operation.

Pixel Sensors

The pixel detector’s sensor and chip design is described in detail in [42, 60]. The pixel sensors are processed in planar technology, *n-in-n* (*n+* pixelated implants on *n*-bulk). The *n*-bulk is oxygenated to reduce acceptor creation during irradiation thereby reducing final depletion voltage as proposed by the RD50 collaboration. In this design, electrons are collected and the high field side will reside, after type inversion, on the pixel side enabling an under-depleted operation with less signal.⁷ There are two methods to guarantee pixel isolation, namely *p+* spray for the barrel pixel and a *p+* stop design for the forward pixel. Guard rings on the edge of the

⁶ With an initially lower luminosity an integral fluence of $\Phi_{eq} = 6 \cdot 10^{14} n_1 \text{ MeV}/\text{cm}^2$ is expected after 4 to 5 years of initial running.

⁷ In *n-in-n* under-depletion mode, the non-depleted zone stays on the backside only reducing the active volume but with depletion zone at the segmented pixel face.

sensors, being kept on relative ground, guarantee a stable running up to bias voltages of 600 V without breakdown. Test beam runs [136] with un-irradiated and irradiated detectors have shown that the barrel sensors still have 99.0% efficiency for tracking charged particles after an exposure of $\Phi_{eq} = 3 \cdot 10^{14} n_1 \text{ MeV/cm}^2$ and the forward sensors maintained an efficiency of 98.8% after $\Phi_{eq} = 8 \cdot 10^{14} n_1 \text{ MeV/cm}^2$.

Strip Sensors

All silicon strip sensors are single sided with AC-coupled readout and $p+$ strips biased through polysilicon resistors, based on the planar process. Pitches range from 80 to 183 μm without any intermediate strips. The substrate is non-oxygenated float-zone n -type silicon made from 6 in. diameter wafers. All barrel sensors are consequently rectangular with strips running parallel to the beam axis, a stereo angle for layers 1, 2, 5 and 6 is achieved by rotating the complete sensor inside the module by 100 mrad. All sensors in the forward part are trapezoidal with strips running in the radial detector direction. As discussed earlier outer modules contain two daisy-chained sensors. In order to maintain a good signal-to-noise ratio of well above 10 (after irradiation) CMS uses thicker silicon sensors for the outer tracker region (500 μm thickness as opposed to the 320 μm in the inner tracker) with correspondingly higher signal. These thicker sensors would in principle have a higher depletion voltage, since $V_{FD} \propto D^2$. But since the radiation levels in the outer tracker are smaller, a higher initial resistivity can be chosen such that the initial depletion voltages of thick and thin sensors are in the same range of 100–300 V, since $V_{FD} \propto N_{eff}$. The different sensor parameters, electrical as well as geometrical, are presented in Table 5.1. The load capacitance is the main source of noise for fast signal shaping, therefore detailed studies were conducted to establish a correlation between pitch p , strip width w , sensor thickness D and load capacitance composed of inter-strip and backplane capacitance. Multi-geometry sensors were processed in the R&D framework of CMS together with the vendor where several combinations of w/p were tested on $\langle 111 \rangle$ silicon crystal orientation as well as $\langle 100 \rangle$ silicon, as well as for different resistivities. The result proved that for a constant w/p the total capacitance C_{tot} stays constant, inter-strip capacitance decreases in the same order as backplane capacitance increases (see Fig. 5.15). Furthermore, to achieve robust coupling capacitors a multi-layer dielectric was used. A good process stability of polysilicon resistors was achieved by saturating by heavily doping the sheet resistance. Further information about the CMS sensor design can be found in [24, 32, 52, 53]. Formulas (5.1)–(5.3) parameterize the results

$$C_{int} = \left[0.03 + 1.62 \frac{w + 20\mu\text{m}}{p} \right] \frac{\text{pF}}{\text{cm}} \quad (5.1)$$

$$C_{back} = \epsilon_0 \epsilon_{Si} \frac{p}{D} \frac{1}{1 + \frac{p}{D} f(\frac{w}{p})} \quad (5.2)$$

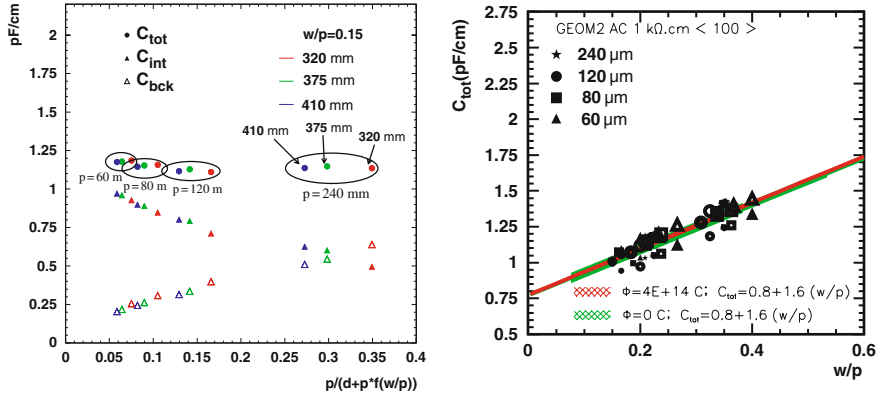


Fig. 5.15 Varying width and pitch of the microstrip sensor, CMS finds a constant total capacitance for a constant width/pitch (w/p) ratio. The left plot shows the constancy of C_{tot} together with its two components C_{int} and C_{back} for a constant $w/p = 0.15$, capacitances are plotted vs. formula (5.2). The right plot shows the linear increase of C_{tot} with increasing w/p . The test holds true for several sensor thicknesses and for $\langle 111 \rangle$ as well as $\langle 100 \rangle$, but only $\langle 100 \rangle$ shows also robustness vs. radiation, refer also to Fig. 5.19 and [24, 32, 52, 53]

$$C_{tot} = \left(0.83 + 1.67 \frac{w}{p} \right) \frac{\text{pF}}{\text{cm}} \quad (5.3)$$

A constant $w/p = 0.25$ is used for all CMS sensors resulting in a load capacitance of 1.2 pF/cm strip length.

Within the high radiation environment of LHC all sensors will undergo type inversion, as discussed in Sect. 1.10. The main strategies of CMS to ensure radiation hardness of silicon sensors consist of

1. delaying the bulk type inversion and achieve V_{FD} always below 400–500 V
2. the use of stable sensors with respect to high voltage and
3. the reduction of surface damage

Delaying Type Inversion – Guarantee $V_{FD} < 400\text{--}500$ V

A tailoring of sensors and of the operation plus maintenance scenario is possible to withstand a substantial amount of radiation by taking into account all theory (see also Sect. 1.10) of radiation damage. Especially important is the evolution of full depletion voltage vs. fluence, time and temperature. The three main strategies are the following:

- freeze out all reverse annealing by maintaining all sensors at sub-zero temperatures during operation and mainly maintenance
- exploit beneficial annealing with a controlled warm up during the maintenance periods
- start with relatively low resistivity silicon to reach the inversion time late and end with about the same depletion voltage as the initial one

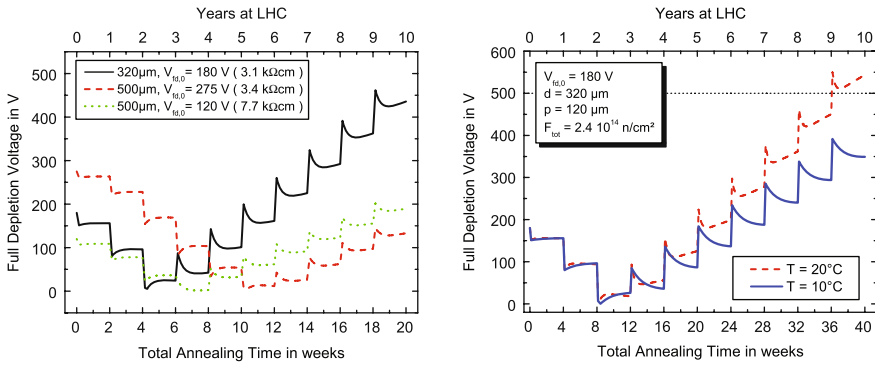


Fig. 5.16 The CMS sensors are subjected to a high radiation field. To freeze the radiation damage and to decrease leakage current the operation temperature is -15°C . During shutdown and maintenance periods the tracker will be “warmed up” for required interventions or to make controlled use of the beneficial annealing effect (see Sect. 1.10.1) [55]

The employment of low resistivity silicon and therefore high initial V_{FD} delays the type inversion point in time resulting in an operational depletion voltage after 10 years of LHC operation. Figure 5.16 (left part) shows the simulated evolution of V_{FD} with time including all operation and maintenance periods, hence radiation and annealing periods. The different time constants for beneficial and reverse annealing have to be exploited. During operation at -15°C all defect annealing processes are suppressed. Operating at low temperature is also necessary to limit leakage current and avoid thermal runaway. During maintenance periods the tracker will be “warmed up” to benefit from the beneficial annealing component. Figure 5.16 (right part) shows the resulting depletion voltages depending on the “warm up” temperatures and it clearly shows that these periods are needed, but with meticulous temperature control. During the whole production period, sensors and test structures have been irradiated and results were compared to the Hamburg model – Fig. 5.17.

High Voltage Robustness

As a second measure, the sensors have to be extremely robust with respect to operation voltage. For several regions, bias voltages of around 500 V will be necessary after 10 years of LHC operation. The basic strategy is to shift high fields into the isolation oxide and consequently avoid high local fields:

- all implants are deep and round shaped
- no sharp corner on any metal structure, only rounded shapes
- active $n++$ edge to have a defined homogenous field at the outer region
- no chips/breaks larger than $\pm 20\mu\text{m}$ at the cut edges, not penetrating the active edge

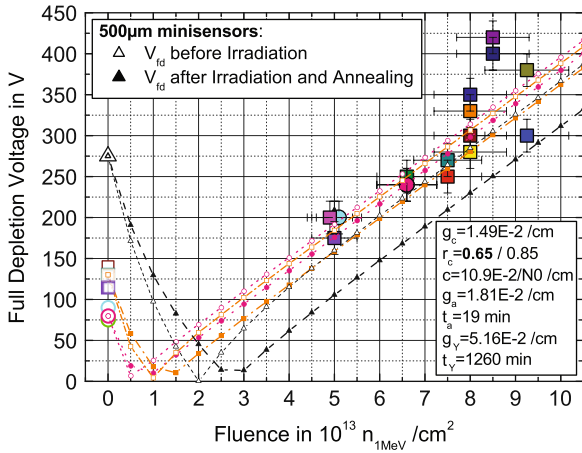


Fig. 5.17 Depletion voltages of several CMS sensors for several fluences. These measurements were used to determine the Hamburg model (see Sect. 1.10.1) parameters for the CMS sensors and to evaluate operation parameters during the 10 years running period [55]

- metal overhang to distribute field to the SiO_2 –metal region for strips, guard and bias ring
- implementation of a floating guard ring with a metal overhang to continuously smooth the high potential (HV) from the edges to GND applied on the inner bias ring. This is an improved version of a multi-guard ring which levels the potential discretely
- after type inversion, high field region is located at the sensor backplane

The use of round structures and avoidance of breaks and chips together with an active edge⁸ are more or less standard methods to avoid any high local field. The implementation of a metal overhang is a CMS innovation and improves voltage robustness significantly. High fields⁹ at the $p+$ implants were shifted towards the metal strips into the SiO_2 insulation where the breakdown voltage is 20 times higher ($V_{\text{break}}(\text{Si}) = 30 \text{ V}/\mu\text{m}$, $V_{\text{break}}(\text{SiO}_2) = 600 \text{ V}/\mu\text{m}$). In addition, it was possible to reduce a multi-guard ring to a single one with an overhang operating with a continuous potential shift of the high voltage at the sensor edge to GND at the bias ring. Many layout simulations and final testing of the implementation was necessary. The metal overhang ranges between 4 and 8 μm . At best, the aluminium electrode should even have a slightly more negative potential than the $p+$ implant. All sensors were tested during standard quality control up to 550 V, many up to 800 V and some sensors were tested even up to 1500 V without breakdown.

⁸ Was already implemented in CDF II, refer to Sects. 1.6.2 and 4.3.

⁹ Main field from the high bias voltage applied to reverse bias the pn -junction.

Surface Damage Reduction

As a third measure CMS uses $\langle 100 \rangle$ with less dangling bonds than standard $\langle 111 \rangle$ silicon (Fig. 5.18). Formula (5.4) lists the surface density of dangling bonds.

$$\text{Surface density} \begin{matrix} 11.8 \\ 9.6 \\ 6.8 \end{matrix} \times 10^{11} \frac{\text{atoms}}{\text{cm}^2} \begin{matrix} \langle 111 \rangle \\ \langle 110 \rangle \\ \langle 100 \rangle \end{matrix} \quad (5.4)$$

The use of $\langle 100 \rangle$ with the lowest number of dangling bonds naturally leads to a suppression of surface damage resulting in reduced increase of inter-strip capacitance after irradiation. Figure 5.19 illustrates the capacitance differences of radiated $\langle 111 \rangle$ and $\langle 100 \rangle$ sensors. In addition the use of $\langle 100 \rangle$ also decreases the undesired oxide charges therefore decreasing micro-discharge probability (Sect. 1.6.3).

The interested reader will find more exhaustive information about the CMS sensors and their quality control program in [9, 79, 105]. The process control, a vital part of the quality assurance, is described in detail in [25, 114].

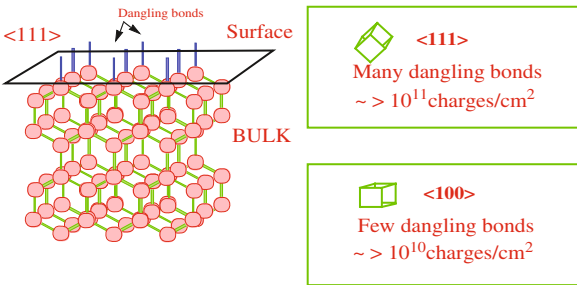


Fig. 5.18 CMS uses $\langle 100 \rangle$ instead of $\langle 111 \rangle$ crystal orientation, exploiting the smaller number of dangling bonds at the Si-SiO₂ interface allowing less charge accumulation due to irradiation

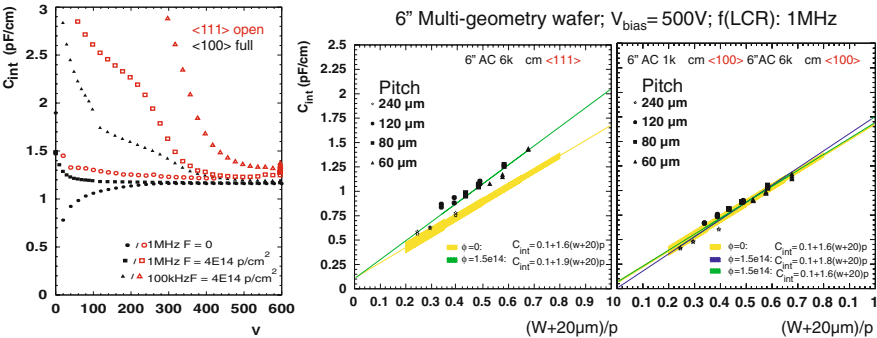


Fig. 5.19 In the *left part*, the full bullets show the beneficial effect of $\langle 100 \rangle$ crystal orientation. Differences at over-depletion are better seen in the *right part*. The study is consistent for several different pitches and strip widths. A clear beneficial effect of the $\langle 100 \rangle$ orientation is shown [24, 32, 52, 53]

The following items summarize the CMS tracker strategies to guarantee a safe 10 year operation:

- relatively “low” silicon resistivity is used resulting in high initial depletion voltage shifting type inversion to a later time ending up with voltages that are not too high
- operation at low temperatures limits leakage currents, avoids thermal runaway and freezes reverse annealing
 - to freeze the reverse annealing, the detector must remain cold, also in the maintenance periods
- the beneficial annealing effect is exploited by a controlled temperature rise during shutdown periods
- voltage robustness of the sensors is improved to allow for high voltage running especially with the use of a metal overhang design
- $\langle 100 \rangle$ silicon was chosen to minimize $Si-SiO_2$ interface deterioration

Figure 5.20 depicts the estimated functionality over the complete operation period of the CMS tracker with higher than marginal signal/noise ratio. All sensors are operational at 400 V and above, a clear sign of a successful design. A number of modules were thoroughly tested for beam incident robustness which they passed successfully, refer to [62, 63, 80].

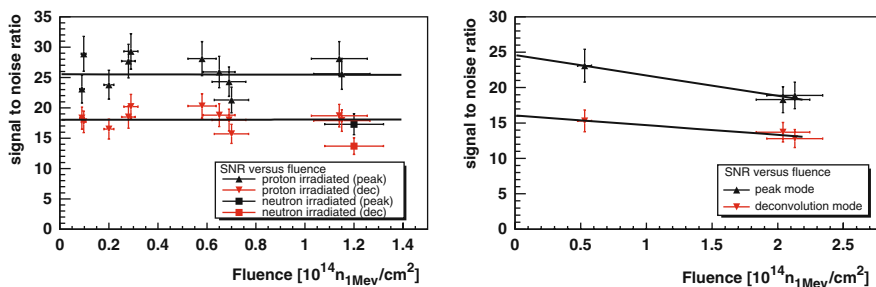


Fig. 5.20 Signal/noise of full CMS modules after neutron and proton irradiation (right plot: protons only). The values far exceed the expectation and technical design specification. [162]. A substantial number of full modules were irradiated to several fluences to guarantee full functionality for the 10 years of operation with a sufficient signal/noise value

The Thermal Screen

To guarantee the sub-zero temperature described above during the whole operation and maintenance period of 10 years, an active thermal screen was designed and built. This is an innovative and unprecedented feature of a tracking detector. The thermal screen is an “intelligent” insulation, responsible to keep the inside below -10°C and the outside at $18 \pm 1^\circ\text{C}$. This is achieved with 32 cold panels inside a Rohacell

insulation layer and several dedicated heating foils outside. Two dedicated cooling stations guarantee the cold operation, while the heating foils are controlled by a dedicated system via PID¹⁰ feedback loops. This engineering masterpiece is one of the keys for the silicon sensor to survive in the harsh environment. The thermal screen is located inside the tracker support tube surrounding the TOB and TEC sub detectors.

5.2 Construction Issues for Large Detector Systems with Industry Involvement

Describing all the logistics, quality assurance steps, technology choices, failure description, etc. of the CMS tracker could fill a book by itself and is the subject of a larger number of publications and conference presentations, e.g. [8, 49, 80, 84, 141]. The challenge to equip 206 m² with silicon detectors up to radii of $R = 110$ cm is unprecedented. The achievement was made possible by adopting and developing new production and quality assurance methods and adapting industrial techniques. These procedures were novel in the field of particle physics detectors. A large collaboration of 51 institutes with almost 500 physicists and engineers succeeded over a period of 12–15 years to design, develop and build this unique device.

Table 5.2 presents an example of the numbers of components and Fig. 5.21 visualizes the different locations, distributed all over the world, of the different assembly levels. In between every shipment there are defined acceptance protocols, e.g. visual

Table 5.2 Number of individual components built into the CMS strip tracker

Thick sensors	18192
Thin sensors	6052
Front-end hybrids/full modules	15232
FE ASICs	75376
Electronic channels	9316352
Petals	288
Rods	688
Analog optical links for 65 m transm.	>40000
Front-End Drivers (ADC boards)	440
Peak module assembly per day	90
Optical fibres	3000 km
Voltage channels (LV + HV)	8000
Temperature and humidity sensors	1000
Slow control computer	10

To stress the fact even a bit more, a petal consists of about 400 sub parts each, a module has about 10 items with about 1000 to 3000 wire-bond connections. A hybrid has 4–6 chips in combination with three additional ASICs and about 40 passive components.

¹⁰ Proportional plus *Integral* plus *Derivative* (PID) control, an industry control standard.

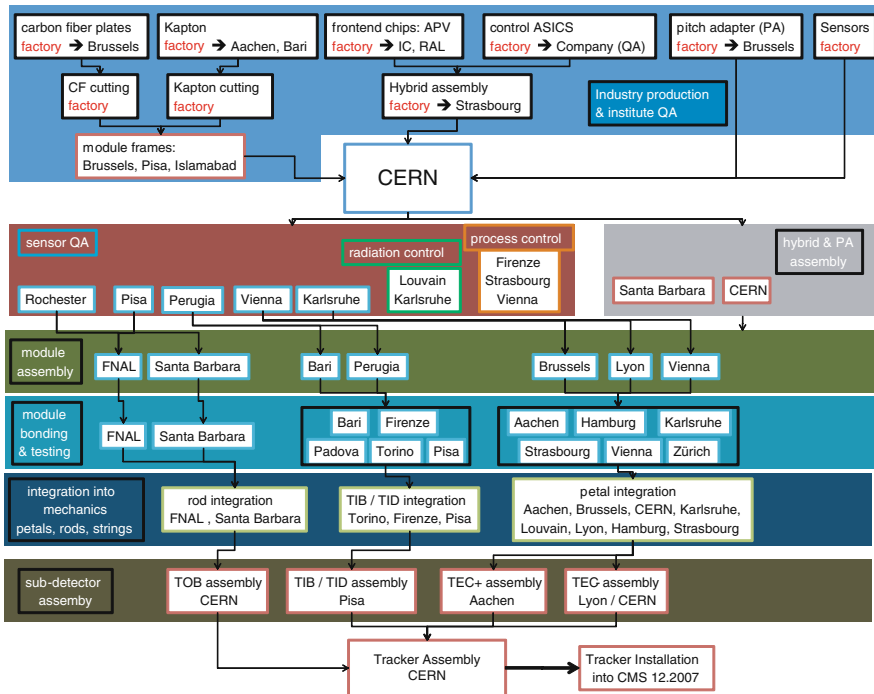


Fig. 5.21 The CMS tracker logistics

inspection and/or electrical testing. Also in between each assembly step a quality assurance test is mandatory. A consequence of the increase in detector size is a change in the personal attitude towards the individual sensors and modules. With the number of sensors exceeding several thousand elements these have to be tested, handled and used in a nearly industrial manner. The time is over when each individual silicon sensor received special attention and was “brought to life” in many hours of careful handling. The silicon detector community had to develop standard procedures to systematically test sensors, efficiently perform the module construction and to use them in large detector systems.

5.2.1 Quality Assurance and Problems During the Process

A detector of this size and complexity calls for unprecedented meticulous quality control to identify and solve problems as early as possible in the production. Some examples are listed. Basic *quality assurance* (QA) strategies for silicon sensors are described in Sect. 1.7.1 including the steps introduced for CMS. In addition to the standard sensor quality control, CMS introduced a special “process monitoring” necessary for the long procurement time of 3 years for the sensors. Due to

the stringent radiation requirements a fraction of sensors and test structures were irradiated to 1.5 times the nominal fluence levels. The result is an overall percentage of good strips in the accepted sensors of 99.94%. The early qualification steps are described in [9, 79]. Along the way all kinds of faults were encountered and all were subsequently solved, mostly in close collaboration with the vendor. In an early stage of delivery coupling capacitors consisted only of SiO_2 . This insulation layer technique proved to be fragile and several pinholes developed during initial quality control. The issue was solved with the introduction of additional layers of nitride [105]. The stringent requirement of cut edge breaks/chips below $20\text{ }\mu\text{m}$ required several visits to one company to sensitize them to the problem. The thin sensor handling plus requested measurements “after” cutting was not a common standard for the manufacturer. Also scratches occurring on certain areas of the sensor was a frequent fault. On a wafer with 100 ASICs a scratch decreases the yield by a percentage but with a single sensor per wafer the yield drops to zero. Testing personnel were finally specially trained for our requirements, see also. Sect. 1.13 and [36, 80, 105]. In Sect. 1.13 a short description of the low inter-strip resistance problem is presented. The problem was identified due to vigilance and the stringent process monitoring established, because inter-strip resistance is not a standard QA item of the manufacturer.

For a period of about 2 months a high flat-band voltage was experienced due to oxide contamination, oxide traps and/or interface states for a large quantity of sensors – $\sim 1,000$ sensors. An immediate irradiation campaign showed a resulting increase of inter-strip capacitance with radiation different to the non-contaminated $\langle 100 \rangle$ sensors [114].

Very prominent was the finding of corrosion of the aluminium bias and guard rings, described in Sect. 1.13 and elaborated in detail in [81].

Even after sensor QA individual channels exhibited an influence on common mode noise due to micro-discharges, observed in the module long-term testing. A single strip, inconspicuous during sensor QA, was able to significantly increase the noise of a full chip [36]. An additional voltage¹¹ had to be applied to the AC pad, while current was measured on the DC pad to mimic the operation condition in a module. In this configuration a strip vulnerable to micro-discharge exhibited a significantly higher current.

Glass pitch adapter series were delivered with varying metal line quality and bonding was not always possible. The ability of sensors and pitch adapters to be bonded was constantly monitored during the whole production. The final bonding failure rate stayed below 0.01%.

Another serious problem affected a series of hybrids. Vias were unstable under thermal stress. A cleaning step during processing was also etching part of the glue between the Kapton layers. The metal conductor path was therefore stretching too far into the grooves and was breaking under thermal expansion. As a solution, an additional Kapton layer was introduced and the via size was increased, see also [58, 84, 104].

¹¹ During operation together with the hybrid, the potential on the chip connections are $+0.85\text{ V}$ higher than the sensor ground.

A new problem relevant only for sensors in a very high-radiation environment was detected during module production. The back side module contact was made with conductive glue between aluminium sensor backplane and metallized Kapton. Varying and aging conductivity of the conductive glue were found between several Ω and several $k\Omega$. Oxygen was diffused through the glue oxidating the aluminium surface and thus degrading conductivity. For a sensor with bulk resistance in the order of several $G\Omega$, an additional series resistance of some $k\Omega$ is of no consequence at all. Since the bulk resistance drops significantly with radiation down to several $k\Omega$, the voltage drop on the glue would be in the same order as for the sensor bulk and depletion could no longer be guaranteed [58, 84, 104]. All modules were therefore retrofitted with backplane bonding.

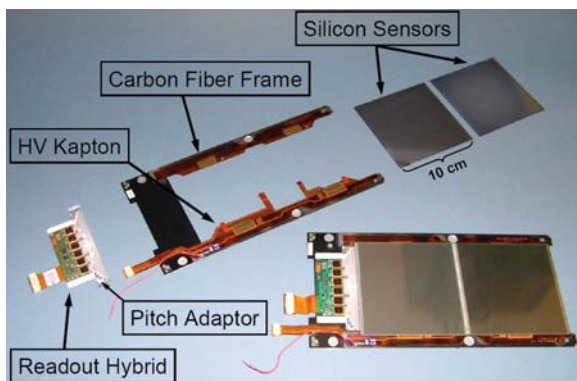
The prior mentioned active $n++$ edge introduces the feature that the edge is at a high potential and therefore wire-bonding with a low loop height resulted in a voltage spark. Module quality control detected this problem and bonding loop parameters had to be adapted accordingly.

All components, hybrids, modules, rods, petals and sub detectors, were long-term tested and all went through several thermal cycles. The level of quality assurance was new for the HEP community but ultimately with zero fault tolerance and rigid vigilance, the final strip inefficiency remains below 0.5%. This includes all sensor, chip, hybrid and module faults and all missing connections from readout and power towards the tracker.

5.2.2 Assembly

To realize a tracker composed of 1440 pixel and 15232 strip detector modules, industrial quality control and assembly methods and logistic structures are necessary as well as a modular design. The smallest assembled element is a module, an example is shown in Fig. 5.22. Modules were assembled in six institutes worldwide using automated robotic “gantry” systems. A gantry system consists of a camera surveying the various components, a robotic arm which can hold vacuum pickup tools for placing sensors and hybrids and syringes to precisely dispense silicone

Fig. 5.22 A CMS module. The different parts forming a module are the frame of carbon fibre and Kapton, the hybrid with the front-end electronics and pitch adapter and the silicon sensors. Courtesy of colleagues from UCSB Santa Barbara, California



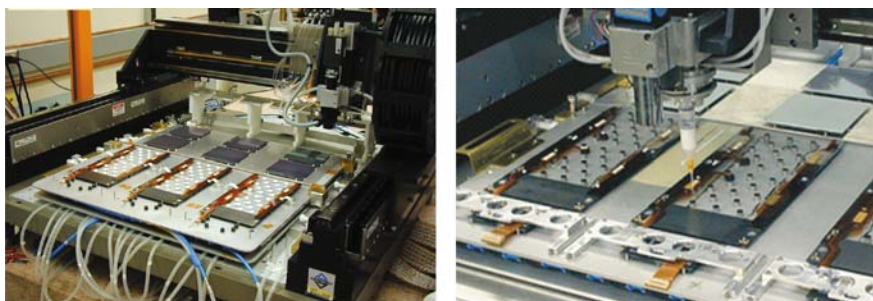


Fig. 5.23 The gantry is a robotic assembly for modules. The gantry systems consist of a camera surveying the various components, a robotic arm which can hold vacuum pickup tools for placing sensors and hybrids and syringes to precisely dispense silicone epoxies

epoxies. Pitch adapter to hybrid assembly was also fully automated on a gantry. A CMS gantry is shown in Fig. 5.23. With pattern recognition a precision placement of $10\mu\text{m}$ and 0.1 mrad was achieved. A removable assembly plate holds components for three or four modules. After the assembly, the plates were moved, with module components fixed by vacuum, to complete the curing of the glue, while the gantry was available for further assembly work. With this procedure a worldwide peak assembly rate of 90 modules/day was achieved. Modules were then sent to bonding centres with high-throughput industrial bonding machines. Bond pictures are displayed in Fig. 5.24; 25 million custom wire-bonds were necessary to finish the module construction. As the next step, modules were assembled into TIB strings, TOB rods (Fig. 5.8) and TEC petals (Fig. 5.25) – in the shell, rod, and petal integration centres.

Overall, 7 sensor quality assurance centres, 3 hybrid production sites, 6 module gantry centres, 2 hybrid assembly centres, 13 bonding and module testing centres, 2 rod integration and 7 petal integration centres and 7 shell integration centres struggled through construction and logistics, however they were very successful. CMS has gained experience in logistics of a large production which is widely distributed over several institutes and countries, refer to Fig. 5.21. The petal integration center of Karlsruhe is presented in Fig. 5.26.

The remaining steps were (1) insertion of sub structures into the sub detectors, (2) inserting sub detectors into tracker support tube, (3) installation of the tracker into

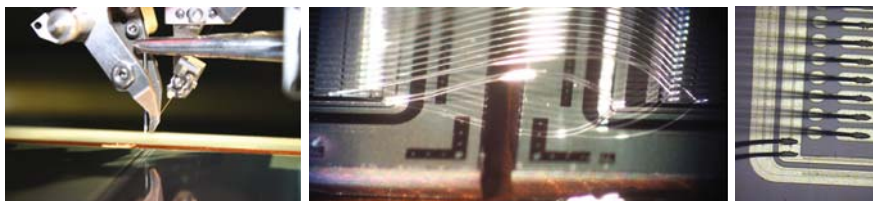


Fig. 5.24 CMS module bonding

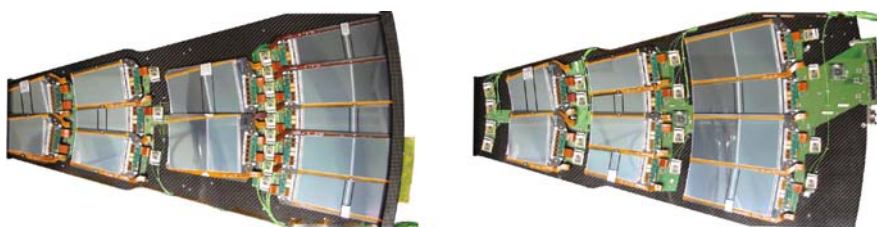


Fig. 5.25 The inner disk petals are the largest of the eight petal types, equipped with 28 modules and more than 1 m long. The pictures show both sides of a petal. All modules are assembled with an overlap and space seen taken by electronics is covered on the other side with modules. A 100% coverage plus overlap is established. All strips are following a full radial path, but some modules are rotated by 100 mrad to have two-dimensional point information. Eight different petal types are needed to cover all cases on the endcap volume. One TEC is composed of 144 petals

the main CMS detector plus (4) the connection of all power cables, optical fibres and cooling pipes.

Rods were integrated into the TOB structure in a drawer-like fashion, see Fig. 5.8. The TOB was then inserted into the tracker support tube, resting on a dedicated rail system.

TIB and TID modules were mounted directly and manually onto the different TIB layers and TID disks. TIB and TID were assembled together with cables, pipes and fibres, integrated then tested and inserted into the TOB, resting on another dedicated rail system, see Fig. 5.9. The picture also shows a fraction of the amount of necessary services to be connected.

Petals were mounted on the front and back side of the nine TEC disks. Insertion happened sectorwise on one disk face only, then the whole TEC was rotated to



Fig. 5.26 Petal integration in Karlsruhe. Three technicians plus two physicists were assembling two petals simultaneously. The petals were mounted on so-called petal grills which enable easy turnaround and thus access to both sides. After assembly, petals were long-term tested in fridges with additional active petal cooling

get easy access to the other disk face. For the TEC all services like fibres, cooling and power cables were integrated even before the first petal was inserted. A sector cabling and petal placement from the front can be seen in Fig. 5.10. The TECs were then inserted into the tracker support tube on the same rail system as the TOB.

Late December 2007, 8 years after the decision to construct an all-silicon tracker, it was finally inserted into CMS, inside the barrel electromagnetic calorimeter. Figure 5.27 catches the historic moment.

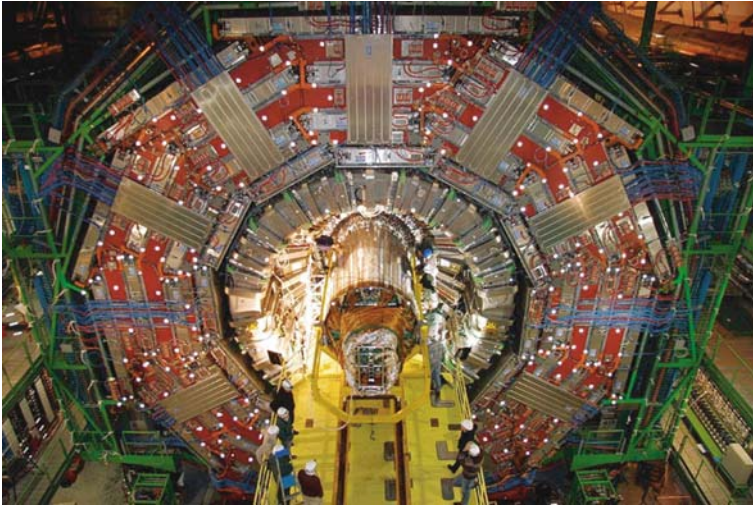


Fig. 5.27 Tracker insertion. After assembly and testing, the CMS tracker arrives in the heart of CMS. From this moment another 3 months were needed to connect all fibres, cooling pipes and power cables before commissioning and data taking was possible. Around 130 km of cables and 18 km of cooling pipes were installed and tested [Courtesy of CERN]

The CMS spokesperson, Tejinder Virdee about the CMS tracker:

Constructing a scientific instrument of this size and complexity, designed to operate at the LHC without intervention for more than ten years, is a major engineering and scientific achievement. More than five hundred scientists and engineers from fifty-one research institutions world-wide have contributed to the success of the project.

The meticulous design and quality assurance paid off. The CMS tracker was installed inside CMS; it was connected and is ready to operate for 10 years. Today, August 2008 about 99.5% of the tracker is working properly.

5.3 Physics with the CMS Tracker and High-Level Trigger

For the high luminosity operation, 1000 tracks of leptons, heavy quarks, corresponding jets plus jets from additionally created mesons – mostly pions – are expected. A simple event is shown in Fig. 5.28.

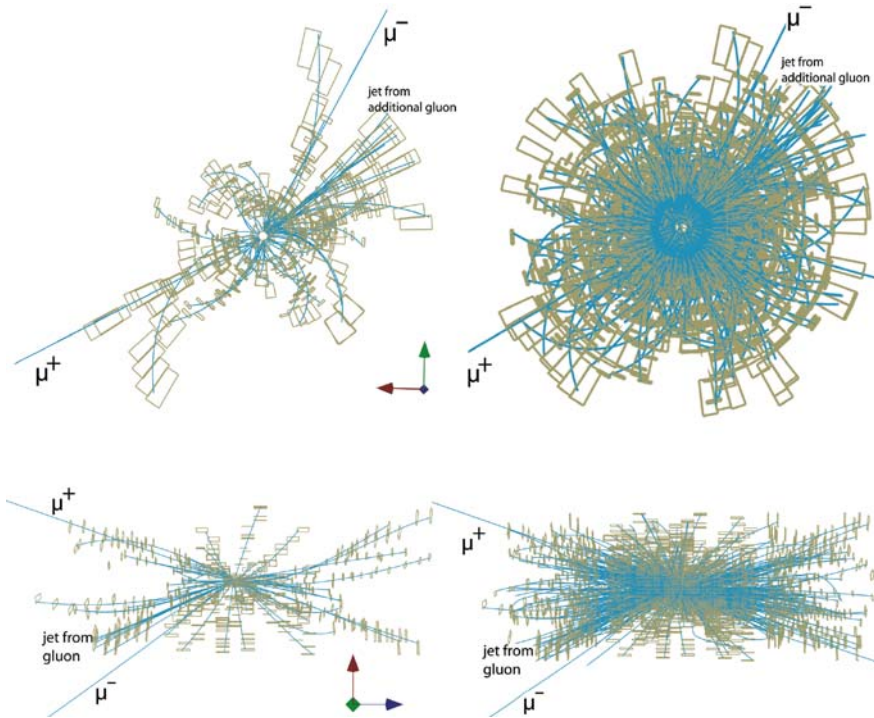


Fig. 5.28 $p\bar{p} \rightarrow Z + X; \quad \hookrightarrow Z \rightarrow \mu^+ \mu^-$ (simulation). The event displayed is a very basic one. As a primary reaction a u quark plus a $\bar{u}$ quark of two protons annihilate to form a Z , subsequently decaying into μ^+ and μ^- . The additional visible tracks are particles (mostly pions) from additional soft processes of gluons and other quarks of the two protons. The left picture shows the bare event. The right displays the same event with five additional minimum bias events from soft processes of other proton pairs. Below, the same event is shown from another angle. At high luminosity operation about 20 minimum bias events are expected. About 1000 additional tracks are expected

Interesting physics signals are many orders of magnitude less frequent than background events! Cross sections vary over many orders of magnitude where physics processes have to be extracted:

- inelastic: 10^9 Hz
- $b\bar{b}$ production: 10^6 – 10^7 Hz
- $W \rightarrow l\nu$: 10^2 Hz
- $t\bar{t}$ production: 10 Hz
- Higgs ($100 \text{ GeV}/c^2$): 0.1 Hz
- Higgs ($600 \text{ GeV}/c^2$): 0.01 Hz

The tracker is essential not only to reconstruct charged particles and measure their momentum but also for *High Level Trigger* (HLT), lepton identification (μ and e), b and τ tagging; also energy flow (jet reconstruction) in the full energy range. In combination with the muon detection system and the calorimeters, the CMS tracker

substantially improves momentum and energy resolution. Track isolation cuts can, for example, distinguish between muons coming from jets or from heavy objects. The CMS tracker is also ultimately necessary for all analyses to precisely reconstruct the primary vertex in full reconstruction.

Tracker Contributions to Precision Measurements

Several parameter determinations cannot be attributed to a single CMS sub detector. The following paragraphs introduce the tracker contribution to muon reconstruction and electron energy determination as examples. A full overview of the CMS detector's physics performance can be found in [43].

Contribution to Muon Reconstruction

A basic strength of the CM(uon)S detector is the reconstruction of muons, where the muon stations together with the tracker and calorimeter are combined in the energy flow concept. In the *global reconstruction* muon trajectories are extrapolated into the tracker volume, where the energy loss in the material plus multiple scattering is taken into account. The tracker measurements improve the transverse momentum resolution at lower energies. Figure 5.29 shows the global muon $p_{\perp}$ resolution.

A complementary algorithm to the *global reconstruction* is the *muon identification*. All tracks in the silicon tracker are quantified vs. a muon compatibility hypothesis. All available information is taken into account including energy loss in the tracker and associated energy deposited in the calorimeters. This method allows the identification of low $p_{\perp}$ muons not reaching the outer muon layers. *Muon identification* adds about 10% to muon detection efficiency with respect to standalone *muon reconstruction*. The combination of both reconstruction algorithms enhances statistical samples of events containing multiple muons (e.g. $H \rightarrow ZZ^* \rightarrow \mu^+ \mu^- \mu^+ \mu^-$).

The tracker together with the calorimeters also significantly contributes to the muon isolation analysis for low $p_{\perp}$ muons. Muons originating from b , c , K or π decays are accompanied by particles from the associated jet. Muons from heavy objects W , Z are more isolated. If the deposited energy in a defined cone around the muon is lower than a certain threshold, the muon is considered isolated – the deposited energy is determined by transverse energy in the calorimeter or sum of transverse momenta of reconstructed particle tracks. The muon isolation (jet/no jet) helps to distinguish between muons of heavy objects or muons produced in jets.

Contribution to Electron and Photon Reconstruction

As for the muons, the tracker improves the ECAL selection of prompt electrons and photons by applying an isolation criteria. To distinguish prompt photons and electrons from those produced in a jet, the summed energy deposited in a cone

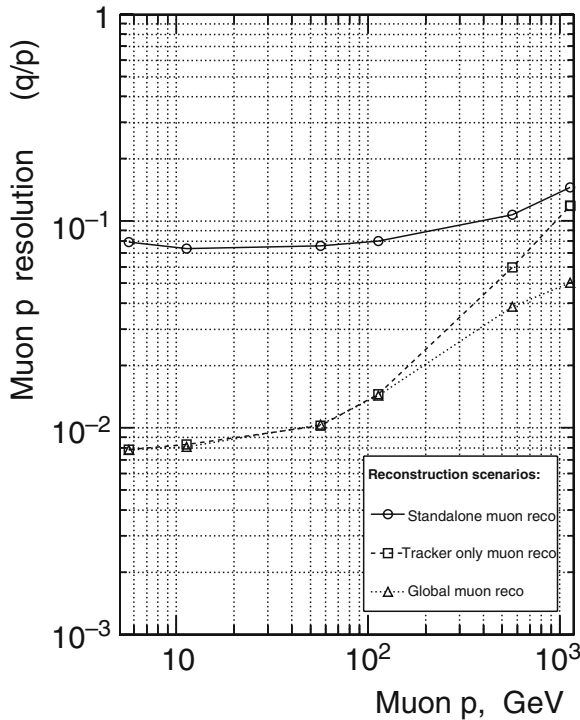


Fig. 5.29 Global muon $p_{\perp}$ resolution. Up to energies of 1 TeV, the transverse momentum resolution of a muon is dominated by the tracker, while at higher energies, the multiple scattering term is less significant and the larger lever arm of the muon chambers improves resolution [43]

around the identified electron or photon must remain below a defined threshold. For an electron, in addition, the reconstructed energy in the ECAL must match the reconstructed track momentum of the tracker. The isolation algorithm improves background reduction for the channels $H \rightarrow ZZ^* \rightarrow e^+e^-e^+e^-$ and $H \rightarrow \gamma\gamma$, where isolated electrons or photons are expected.

The tracker also improves the precision on the electron energy measurement in a certain range, through the high precision $p_{\perp}$ measurement. Figure 5.30 shows the relative energy resolution for electrons measured by ECAL and tracker.

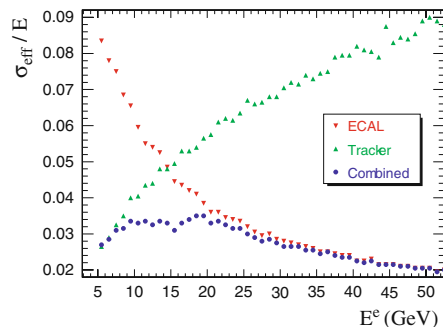


Fig. 5.30 Electron energy measurement. The plot shows the relative electron energy resolution σ_{eff}/E , as measured with the CMS tracker, ECAL and the combined value [43]

High-Level Trigger

Another key role is the tracker’s extensive usage in the *High Level Trigger* (HLT) for all physics event streams [143]. The level 1 trigger system is based on custom electronics and reduces the input rate of 10^9 interactions every second by a factor of 10000–100 kHz. The level 1 decision must be made in $3.6\,\mu\text{s}$, corresponding to the maximum storage capacity on the front-end chips. The HLT, a software trigger, relies on commercial processors and reduces the stored data by another factor of 1000 down to 100 Hz. While the tracker is not participating in the level 1 decision it plays an important role in the HLT. Simplified and faster versions of the full track reconstruction algorithms, with reduced accuracy, are used in the HLT. The two basic principles are

- “*regional tracking*”: The HLT track reconstruction is restricted to the *Region(s) of Interest* (RoI), which is defined by the signal from the level 1 triggers from the muon and calorimeter systems. The transverse momentum $p_\perp$ can be calculated with only a partial track, since it does not significantly¹² change up to the end of the track.
- “*conditional tracking*”: Cuts that stop reconstruction during event selection are introduced, like “momentum is definitively above or below threshold”, “N good hits found”. Often four or six space points are enough for track reconstruction.

These fast reconstructions subsequently allow general $p_\perp$ cuts, defined by physics requirements (physics momentum cuts are for example 0.9 GeV for b tagging or up to 20 GeV for muons). Low momentum coiled tracks are not reconstructed.

As an example a b jet HLT trigger takes a level 1 trigger from the calorimeter (jet), the track seed for conditional track reconstruction is created around the level 1 jet direction. Tracks are solely reconstructed in a cone (RoI) of $\Delta R < 0.15$ around the jet direction. This makes a jet direction refinement possible, to distinguish if it comes from the primary vertex or not.

A second example is the τ trigger. A narrow jet in the calorimeter defines the RoI – cone around a jet. The τ hypothesis requires an associated isolated track to the jet. Conditional and regional tracking in the RoI is performed. The τ hypothesis is falsified if no track is found in a narrow cone around the jet (signal cone) or an additional track is found in a second broader cone (isolation cone) – *regional tracking*. To save CPU time, the track is not fully reconstructed and only a loose primary vertex association is requested – *conditional tracking*. Later at the offline stage, the full track and decay vertices are reconstructed. To reconstruct a full “good” track, the track seed plus five helix parameters (two positions, two angles plus curvature) have to be determined.

Some Examples

With introductory remarks some cases with significant CMS tracker impact are listed:

¹² Except for electrons – Bremsstrahlung.

- the key component for the B physics program is the ability of secondary vertex reconstruction also at HLT level with conditional tracking for processes like exclusive B -decays
 - $B_s \rightarrow \mu^- \mu^+$ and $B_s \rightarrow \mu^- \mu^+ K^- K^+$
flavour changing neutral current ($b \rightarrow s$ loop-level processes)
 - $B_s \rightarrow J\Psi\Phi$
Gold-plated CP violation decay mode sensitive to new physics
- the LHC is deemed to allow Higgs discovery in the full mass range up to 1 TeV
Examining the decay products, one realizes immediately that lepton id , b tagging and missing energy resolution are crucial
 b tagging is especially crucial to reduce background
 - $ttH \rightarrow ttbb$: A very challenging topology where b and lepton tagging is necessary plus a final full reconstruction of e.g. $bbbbqql\nu$
 - $H \rightarrow ZZ \rightarrow l^+l^-l^+l^-$ ($l = e, \mu$) tracker improves μ resolution significantly with respect to the muon chambers
 - $H \rightarrow \gamma\gamma$ tracker can help identify the vertex or reject π^0 (jet) but unfortunately for this analysis the high tracker material budget is more a hindrance
- Minimal Super Symmetric Model (MSSM) or SU per SY mmetry (SUSY) in general. b and τ tagging play a key role as well as for full reconstruction as also for HLT
 - the neutral MSSM Higgs is predominantly produced via gluon fusion $gg \rightarrow bbH^0$. Besides $AH \rightarrow bb$ with an enormous background significant channels are $AH \rightarrow \tau\tau$, thus τ tagging is mandatory
 - charged MSSM Higgs production $gg \rightarrow tbH^+$ decays dominantly into tb and $\tau\nu$ where again t , b and τ tagging is important
 - SUSY signatures: Squark and gluino production leads to lepton(s) plus missing energy plus jets. Also here the tracker plays a key role

The CMS tracker is expected to play an essential role to address the full range of physics which can be accessed at the LHC. Standard model physics like b physics, t physics, Standard model Higgs searches, MSSM Higgs searches and SUSY searches are planned. At 14 TeV jets are mostly expected but also the standard candles W , Z , tt . The full detector concept and especially its trigger flexibility must cover all eventualities, new physics possibly waits just around the corner.

Chapter 6

Continuing the Story: Detectors for the SLHC and the ILC

The two main future colliders are currently under discussion, the successor of the Large Hadron Collider (LHC), the Super Large Hadron Collider (SLHC) and the next e^+e^- machine, the International Linear Collider (ILC). The requirements of both colliders and possible detectors are significantly different but also some synergies exist. Figure 6.1 informs about the increase in size over the past 40–50 years, the logarithmic plot behaves Moorelike.¹ The future will tell us where we will go next.

In the next two sections some ideas, plans and current R&D activities will be discussed.

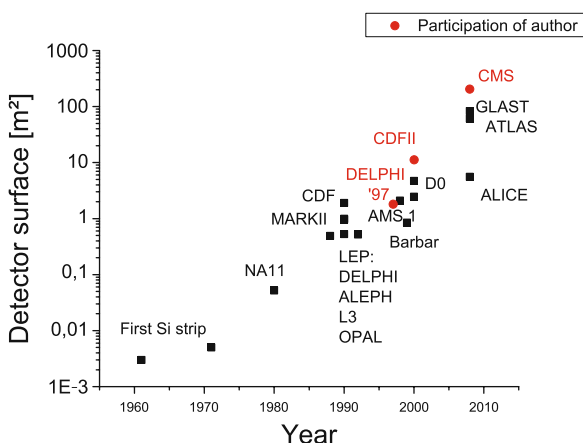


Fig. 6.1 Evolution of silicon detectors – area. In logarithmic scale the plot displays the increase in area for the last 40–50 years. Plotting number of channels and power consumption would result in similar displays. The field is very active. R&D, assembly efforts, quality control plus the related logistics increased a lot in the last years and will even further in the future. To construct a detector with a couple of people over the summer break is no longer possible. Also R&D efforts today are quite diverse as a result of the many new possibilities and needs for the next generation of tracking detectors. Whole R&D-only collaborations exist, e.g. RD50 [160]

¹ According to Gordon E. Moore co-founder of Intel, the number of transistors placed on an integrated circuit increases exponentially, doubling approximately every 2 years. Published in 1965, Moore's law predicts the future of integrated circuits.

6.1 A Silicon Tracker for the Super Large Hadron Collider (SLHC)

For SLHC the peak luminosity will be $\sim 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$, 10 times the peak of the LHC. This has the following implications for the CMS Tracker upgrade: (1) increased radiation and (2) increased occupancy. Also the material budget has to be decreased with respect to the tracker of today, see Fig. 5.12. Powering is also a hot topic, an increase of power has to be avoided, a decrease would be very favourable. Figure 6.2 presents expected fluence after an integrated luminosity of 2500 fb^{-1} at the end of SLHC operation. This of course defines possible technologies vs. radii. The occupancy defining the possible cell size follows the same radial scaling. Pileup can be up to 400 events per crossing. Physics goals demand a detector performance at least as good as the current CMS tracker. For occupancy reasons, the inner parts $5 \text{ cm} < r < 20 \text{ cm}$ will be populated with pixels, for intermediate regions $20 \text{ cm} < r < 50 \text{ cm}$ long strips are no longer an option, therefore long pixels or short strips, STRIXELS, in the order of several millimetres or a few centimetres are envisioned while for the outer region of $r > 50 \text{ cm}$ long strips could still be used. In reality to have a smaller number of sensor geometries, there are ideas to instrument the whole tracker with only pixels and strixels increasing strip channels from 10 million to 1 billion. The current all-silicon-strip-tracker would transform to an all-silicon-pixel-tracker.

As seen in Fig. 6.2 the radiation levels at $R = 5 \text{ cm}$ will be around $\Phi_{eq} = 10^{16} n_1 \text{ MeV/cm}^2$, decreasing to around $\Phi_{eq} = 10^{15} n_1 \text{ MeV/cm}^2$ at $R = 20 \text{ cm}$ while

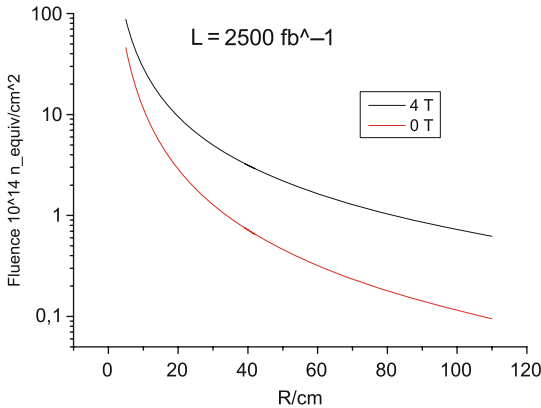
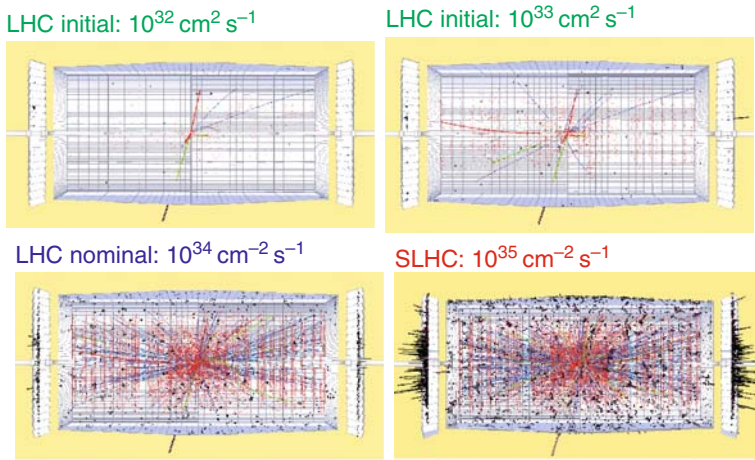


Fig. 6.2 SLHC: radiation vs. radii. The plot presents the expected fluence for SLHC after an integrated luminosity of 2500 fb^{-1} . The distribution underestimates the fluence for larger radii, it takes only charged radiation for the primary interaction into account and neglects backscattered neutron contribution from the calorimeters. The deviation from a $1/r^2$ behaviour derives from the magnetic field responsible for coiled tracks. To achieve a reasonable occupancy it can be imagined to instrument $5 \text{ cm} < r < 20 \text{ cm}$ with pixels, $20 \text{ cm} < r < 50 \text{ cm}$ with strixels and $r > 50 \text{ cm}$ with single standard strip sensor modules

**Fig. 6.3** Event pileup vs. luminosity [157]**Table 6.1** SLHC sensor technology and geometrical layout vs. radius

Radius, cm	Region	Fluence [$n_1 \text{ MeV}/\text{cm}^2$]	Limiting factor	Possible geometry	Possible sensor technology	Comparable solution	Probable
$R > 50$	outer R_1	10^{14}	$I_{leakage}$	strips	strips; $p\text{-on-}n$	CMS TIB	$n\text{-in-}p$ – long strixel
$20 < r < 50$	intermed. R_2	10^{15}	V_{FD}	strixel	pixel; $n\text{-in-}n$ $n\text{-in-}p$	CMS PIXEL	$n\text{-in-}p$ – short strixel
$5 < r < 20$	inner R_3	10^{16}	CCE	pixel		new regime	3D; epi- pixel

at $R = 50 \text{ cm}$ still around $\Phi_{eq} = 2 \times 10^{14} n_1 \text{ MeV}/\text{cm}^2$ has to be endured. The increase in number of tracks due to pileup for the different operation stages of LHC to SLHC is illustrated in Fig. 6.3. Table 6.1 gives an overview about possible sensor technologies, geometric layout and an educated guess as to what will be applied. Radiation levels will be 10 times higher than the current CMS tracker expects, therefore aside from the very inner region R_3 , established technologies like CMS strips (R_1) and CMS pixel (R_2) are sufficient.

That said, there is still room for improvement and homogenization. From RD50, it is known that a high oxygen content suppresses the depletion voltage increase for charged particles fluence. Magnetic Czochralski silicon is naturally and homogeneously oxygen enriched. Furthermore, it is known that p -type material does not type invert. With an $n\text{-in-}p$ sensor the main junction remains on the segmented side and the device can also operate in under-depletion. This is also true

for n -in- n , but without the additional backside guard ring structuring. n -in- p will therefore be cheaper than n -in- n . Recently high resistivity p -type wafers have become available, even grown in magnetic Czochralski (MCz) technique. Due to the electron accumulation layer a n -in- p sensor needs additional strip/stixel isolation structures² – p + stop or p + spray. Electron collection in n -in- p sensors is faster than holes collection in p -in- n sensors, as a drawback, the Lorentz angle is more pronounced. A very important factor is the annealing which for p -type has basically no reverse part. As a reminder CMS used p -in- n technology for strips and n -in- n for the pixel. n -in- p , probably n -in- p (MCz), will naturally work for both purposes with the above-mentioned benefits. Investigations of the different possibilities are ongoing. Additional thinning would also reduce depletion voltage and leakage current thus power ($V_{FD} \sim D^2$; $I_{leakage} \sim D$; $P = PV \sim D^3$). Investigations on 50–200 μm thick wafers are ongoing. The resulting smaller signal ($S \sim D$) is compensated by short strips with lower capacitance, thus lower noise.

For the most inner region (R_3) where trapping is the main problem, standard planar technology on high resistivity floatzone or Czochralski silicon wafers is maybe not sufficient anymore. Here very thin wafers created by epitaxial growth are an option with small capacitance pixels. Other valid candidates are the detectors produced in the new 3D technology with a pixelated geometry, see Sect. 1.11.6.

As an additional global measure, lower temperatures limit leakage currents and more efficient cooling schemes like evaporative CO_2 cooling systems would be beneficial.

An overhaul of electronic ASICs to smaller feature sizes is beneficial because with 130 nm and deeper, enclosed geometry is not needed anymore, the ASICs are radiation tolerant. Also lower voltages are necessarily resulting in a lower power consumption. Many ideas of improvements are under discussion, e.g. longer pipelines, ADCs per channel in 65 nm technology. The smaller feature size allows more features per area. Clearly all new chips have to be tuned to the strip/stixel capacities. Also chips with many channels are under discussion, e.g. 512 or even 1024 channels instead of today's standard of 128 channels.

With the 10-fold increase of luminosity, there is a strong request to incorporate the silicon tracker information into the first-level trigger. The bandwidth for data is limited and a luminosity increase results in higher data rate. Unfortunately a simple increase of existing trigger thresholds is not an option because limits are given by physics and lower limits would cut directly into physics performance. A high $p_\perp$ track trigger is needed for the SLHC running. Ideas about special silicon trigger layers or short straight track stubs are being discussed.

The possible options are still manifold, but the needs are understood. The main challenge is to build an even more efficient tracker with the focus on achieving a lower material budget!

² As does n -in- n .

6.2 A Silicon Tracker for the International Linear Collider (ILC)

A linear e^+e^- collider in the TeV centre-of-mass range is considered to be the next ultimate challenge – the *International Linear Collider* (ILC). At the current time, a lot of speculation about possible detector concepts is under discussion. The one clear fact is that the instrument will be built for precision physics, all detector parameters are driven by physics channels and resolution. The vertex detector must be able to tag b, c, τ decays and hopefully even s quarks. The detector will be operated triggerless, all collisions will be recorded. Detailed proceedings about the vertex detector ideas are presented in [33, 164] while a full overview of ILC detector ideas can be found in [125], a first discussion about strip implementation in [59]. The concept of “particle flow algorithm” is followed throughout the detector, **every** particle must be reconstructed for optimum jet resolution. Therefore the tracker must be able to reconstruct **all** charged particles.

As for the LEP detectors and different from CMS, most of the existing detector concepts³ are incorporating a silicon vertex detector with an outer high precision Time Projection Chamber (TPC). Some pixelated silicon layers (4–5) are planned, maybe additional strip layers as link to the TPC and even outer high-resolution silicon strip layers around the TPC as link to the calorimeter are possible. In all conceptual designs, the use of silicon pixel or strips in the forward direction is planned. Also the TPC readout at the volume end will possibly be realized with silicon sensors or high-resolution gaseous chambers. Design studies and small prototypes exist for a silicon tungsten $Si - W$ calorimeter with $5 \times 5 \text{ mm}^2$ cells and even a digital “tera-pixel” ECAL with $50 \times 50 \mu\text{m}^2$ MAPS readout.

In this section the current vertex detector requirements are discussed plus some promising sensor technology candidates. The future will tell which technology will be chosen.

The requirements are listed below:

- space point resolution of $4 \mu\text{m}$ or better
 - $10 \times 10 \mu\text{m}$ pixels
- impact parameter resolution σ_{d_0} in Rz and $R\phi$ $(5 \mu\text{m})^2 + (10 \mu\text{m}/(p_\perp \sin^{3/2}\Theta))^2$
- a two-track resolution of $40 \mu\text{m}$ or better
- transverse momentum resolution: $\Delta(1/p_\perp) = 5 \times 10^{-5}/\text{GeV}$
- standalone tracking capability
- ultra-low material budget $0.1\% X_0$ radiation length per layer $80^2 + (120/p_\perp)^2$
 - low power consumption
 - gas cooling, crucial to allow low mass construction
 - very light structural elements, e.g. silicon carbon foams

³ Today (2008), there are three concepts: ILD (vertex+Si strips+TPC), 4th concept (vertex+TPC), SiD (vertex+silicon strips).

- hermeticity with special focus on forward geometry
 - full coverage $|\cos\Theta| < 0.98$
- operation in magnetic field up to 5 T
- triggerless operation – particles come in bunch trains
 - fast electronics
 - in situ storage
 - high granularity
 - fast sensor
- moderate radiation tolerance

Unlike a circular electron–positron collider with a constant time interval of beam crossings the ILC will operate with particle bunches organized in trains. In the planned configuration as of today [125] there will be five trains with 2820 bunches per second. The bunches are separated by 307 ns summing to total duration of 0.87 ms resulting in a duty cycle of 1 ms/200 ms. Therefore fast electronics operating in power pulsed mode are necessary, especially with the need to consume very low power to run without active cooling. The triggerless ILC operation together with the dense particle bunches and long trains poses the following requirements on the vertex detector: Detector response must be fast, occupancy must be low to avoid high pileup and detectors must be either read out very fast (e.g. 20 times per train) or signals must be storable in the detector/readout cells. Without a trigger, all signals are read out, therefore sparsification is ultimately needed as well as a pixelated geometry for the vertex detector.

The possible candidates under development are numerous and include (1) Charge-Coupled Devices (CCDs), CPCCD (Column Parallel CCDs), (2) Monolithic Active Pixels (MAPS) based on CMOS technology, (3) DEPFETs (DEpleted P channel Field Effect Transistor), (4) SOI (Silicon on Insulator), (5) ISIS (Image Sensor with In Situ Storage), (6) Hybrid Active Pixel Sensors (HAPS) and 3D integration concepts. The basic technologies are explained in Sect. 1.11 while the devices for the ILC come in several flavours with some specific implementations and also some technology combinations. Standard CCDs as used in digital cameras are not fast enough, proposed column parallel readout CPCCD helps or Short Column Charge-Coupled Device (SCCCD), where a CCD layer and a CMOS readout layer is bump bonded together. Chronopixels are CMOS sensors, with the capability to store the bunch ID (time). ISIS sensors combine CCD and active pixel technology, a CCD-like storage cell together with CMOS readout implemented. Also Flexible Active Pixels (FAPs) integrate storage cells in the traditional MAP cells. Fine Pixel CCDs (FPCCDs) are under discussion to decrease occupancy. To summarize the different varieties of CCDs, DEPFET, MAPS and SOI are designed to read out every 50 μ s, while ISIS and FAPS store signal in cell memory and will be read out in the 199 ms between trains. Also FPCCDs and chronopixels are designed for in-between train readout.

In addition to all the above-discussed technology choices, the requirement to achieve a ultra-low mass tracker demands thin sensors. Methods are under

investigation to either have thin epitaxial sensors like CCD and to thin the other devices. Edgeless processing is under investigation to allow near-adjacent sensor placement instead of traditional staggering; the particle flow algorithm does not allow non-instrumented regions.

New 3D integration technologies are under investigation where two or more thinned layers of semiconductor devices are interconnected to form a monolithic “chip”. In early design concepts, the real sensor together with analog, digital and even optical electronics are vertically integrated in a monolithic circuit. This concept has many obvious advantages and early prototypes are very promising.

The above-mentioned link layers towards the TPC or even surrounding it and also the full silicon tracker will be realized with the strip technology of today, but also here thinning of sensors is under discussion. Also long ladders are planned with “long” strips to achieve a reasonable number of readout channels. Avoiding standard hybrids at the end of modules, second metal routings are discussed with a bump bonding field even on strip sensors and chips with 512 or even 1024 channels are in planning [59]. Double-sided silicon strip sensors are needed to achieve a 2D readout with minimal sensor and structural material.

The rich number of valid technological choices proves the liveliness of the silicon sensor development in the last years.

Chapter 7

Conclusion and Outlook

Reviewing history, collecting experience, looking into the future; an experimentalist in the field of particle and detector physics has to live on the waves of new technologies. As a matter of fact there will always be a new detector with new R&D challenges. The last 20 years of semiconductor devices brought significant progress together with significant science done. Devices have grown 4 orders of magnitude in size, orders of magnitude in readout speed and today, a compensation for 4 orders of magnitude in radiation damage is possible. For larger and larger projects the experts in the field have to always remember what they have learned while utilizing their natural curiosity to invent new lanes. The sensor activity has obvious spin-offs like medical applications and material analysis but we have to sell our science for its content and provide high energy particle physics with its ever-growing needs. This field has a clear natural synergy between particle physics, astroparticle physics, applied physics and condensed matter physics. Silicon detectors with their c -, b - and τ - tagging capability opened a new gate to physics. No other device is able to label jets with their initial content. Candidates for takeover diamond detectors are not yet mature, neither in technological realization nor in cost and will always suffer from the advanced developments of processing in industry. Silicon exists in abundance and is currently the best-known material in the world.

Starting from NA11 with 6 sensors, DELPHI set the next benchmark with 888 detectors followed by CDF with 1752 large area sensors and today CMS leads the record with 24328 sensors from 6 in. wafers, where will we go next? A rich number of technology choices for the next two large HEP instruments – the SLHC and ILC – exists. Independent of which technology will win the race, the field will remain interesting and versatile.

I like to emphasize the past, present and future of particle tracking detectors with the words of two very dear colleagues of mine:

Joe Incandela

I have been very fortunate to be involved in many great silicon detector projects over the years. The CDF projects were all very successful, and provided lots of great physics but they were not as easy as they looked, even when they didn't look that easy. There is no routine way of doing things with large scale silicon detectors. Problems arise at every stage of every project. This has also been true of CMS. The silicon groups I've led and collaborated with over the past nearly 2 decades have included the most dedicated, talented, and hard working

people I have ever known and this is the real reason why we were successful. It's also why the experience has been so memorable.

Manfred Krammer:

The success and advantage in particle physics relies on the rich diversity on detector technologies and their continuous development.

Silicon sensors were, are and will be my favourite field of interest and work.

Glossary

Some Physics Constants and Definitions

HEP: *High Energy Physics* – Collider Physics

Colliders and Detectors

ALICE: *A Large Ion Collider Experiment* at the LHC at CERN, specializing in heavy ion physics [90]

ATLAS: *A Toroidal LHC ApparatuS*, one of the four detectors at the LHC at CERN, counterpart to CMS, a multipurpose detector [15]

CDF: *Collider Detector at Fermilab*, one of the two multipurpose detectors at the TEVATRON

CMS: *Compact Muon Solenoid*, one of the four detectors at the LHC at CERN

D0: Multipurpose detector situated at the interaction D0 at the TEVATRON

DELPHI: *DEtector with Lepton, Photon and Hadron Identification*, on the four multipurpose detectors at LEP

ILC: *International Linear Collider*, a high-energy linear collider in design and planning phase

LEP: *Large Electron Positron Collider* at CERN, operating at CERN from 1988 to 2000. It hosted the ALEPH (*Apparatus for LEP Physics*), DELPHI, L3 (*LEP 3*) and OPAL (*Omni Purpose Apparatus at LEP*) experiments

LHC: *Large Hadron Collider*, proton–proton collider at CERN in Geneva, starting 2008

LHCb: One of the four LHC detectors, specialized on b physics and CP violation.

TEVATRON: The Proton–Antiproton Collider at Fermilab near Chicago, operating since 1983, hosting the CDF and D0 detector

Sub Detectors

ISL: *Intermediate Silicon Layers*; the link silicon detector in between main vertex detector SVX and outer drift chamber COT at the CDF detector

MVD: *Micro Vertex Detector*; innermost silicon strip and pixel vertex detector of DELPHI

SST: Silicon Strip Tracker; silicon strip tracking devices. Abbreviation used in ATLAS and CMS.

SVT: Silicon Vertex Tracker, level two hardware trigger on displaced vertices in the CDF silicon detector

SVX: Silicon Vertex Detector of the CDF detector at Fermilab. Historically, starting with four single-sided layers upgraded to five layer double sided, then named **SVX II**. Also the name of the ASIC readout chip used (SVX to SVX4)

The CMS SST contains the following sub detectors: **TEC**, Tracker Endcap; **TIB**, Tracker Inner Barrel; **TID**, Tracker Inner Disk; and **TOB**, Tracker Outer Barrel

Detector Types

CCD: Charge Coupling Device; another silicon pixelated device, not discussed in this book but very popular in digital cameras

Drift Chamber: Gaseous tracking detector; wires in gas, where wire position plus drift time of ionized electrons and ions define particle position

ECAL: *Electronic Calorimeter*: Measurement device to measure energy of electrons and photons

HCAL: *Hadronic Calorimeter*: Measurement device to measure energy of hadrons, mesons and baryons

RICH: Ring Imaging Čerenkov Counter

TPC: Time Projection Chamber, a gaseous tracking detector, utilizing time/drift information in a large volume for the z-coordinate

Abbreviations for Electronic Chips

APV: Analog Pipeline Voltage. Readout chip in use in the CMS experiment

MX: Microplex used in the LEP experiments, especially in DELPHI. Precursor of the TRIPLEX chip

SVX1–3: Silicon Vertex: chips used in TEVATRON experiments

VLSI: Very Large Scale Integration stands for the process of creating Integrated Circuits (ICs) by combining thousands of transistor-based circuits into a single chip

Abbreviations

CCE: Charge Collection Efficiency

CV & IV: Capacitance or current vs. voltage characteristic – a measurement scan of the global silicon properties

CVD: Chemical Vapour Deposition

DAQ: Data Acquisition

HEP: High Energy Physics – Collider Physics

HLT: High Level Trigger

LCR: Short for a *L*, *C* and *R* metre

MOS: Metal Oxide Semiconductor, in the sensor case mainly aluminium SiO_2 silicon

***b* tag:** The identification of *b* quarks or heavy quark in general

Constants and Formulas

Symbol	Definition	Units or value
c	Speed of light	$2.997924580e^8 \text{ ms}^{-2}$
h	Planck constant	$6.62606896e^{-34} \text{ kgm}^2.\text{s}^{-1}$
μ_0	Permeability of vacuum	$12.566370614e^{-7} \text{ kgms}^{-2}\text{A}^{-2}$
ϵ_0	Permittivity of vacuum	$08.854187817e^{-12} \text{ kg}^{-1}\text{m}^{-3}\text{s}^4\text{A}^{-2}$
N_A	Avogadro's number	6.0221415×10^{23}
$m_e c^2$	Electron Mass $\times c^2$	0.511 MeV
r_e	Classical electron radius	2.818 fm
ϵ_0	Dielectric constant	$8,85 \cdot 10^{-14} \text{ Fcm}^{-1}$
k_B	Boltzmann constant	$1.38065 \cdot 10^{-23} \text{ JK}^{-1}$
e	Electron charge	$1.6 \times 10^{-19} \text{ C}$
β		$\beta = \frac{v}{c}$
γ		$\gamma = \frac{1}{\sqrt{1-\beta^2}}$

V_{FD} : Full depletion voltage, the voltage, where the sensor is just depleted from charge carriers, visible in a kink in the CV characteristic.

V_{bias} : The operating voltage to fully deplete the sensors, $V_{bias} > V_{FD}$.

Pseudo rapidity: $\eta = -\ln(\tan \Theta/2)$ replaces the azimuthal angle Θ and is invariant versus Lorentz addition. In hadron colliders, e.g. CDF and CMS, the z-coordinate of the primary vertex varies. Therefore, the quantity η is used in calculations and also to define and construct the detector elements.

Occupancy: $\phi \times \text{pitch} \times \text{strip length}$.

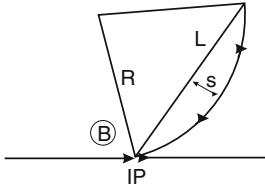
Track, Transverse Momentum Resolution and Impact Parameter Resolution

Track: A helix is a 5D object, defined by two positions, two angles and its curvature. A track state can be represented as a point in 5D linear space. To complete, the track is a measured (fitted) object, and has uncertainties (errors) on it's parameters. A track state is fully described by 5 parameters and a 5×5 symmetric error matrix.

Transverse Momentum Resolution

The momentum resolution of a moving charged particle in a B field is given by its curvature path. With $s = L^2/8R$ and $B \cdot R = p/q$ one gets the momentum resolution as $\frac{\Delta p}{p} \approx \frac{\Delta s[\mu\text{m}]}{(L[\text{cm}])^2 B[\text{T}]} p[\text{GeV}]$. This immediately tells us that (a) intrinsic position resolution has to be good to resolve s and that (b) the B field strength give a linear improvement, while (c) a larger lever arm improves momentum resolution quadratically. With increasing p_T the resolution gets worse again and with an error of 100% the particle charge cannot anymore be identified.

Impact Parameter Resolution: How to design a tracking detector to achieve good impact parameter resolution is illustrated in the following formula:



$$\sigma_{d_0}^2 = \sigma_{MS}^2 + \sigma_{geom}^2 \text{ with } \sigma_{geom}^2 = \left(\frac{\sigma_1 r_2}{r_2 - r_1} \right)^2 + \left(\frac{\sigma_2 r_1}{r_2 - r_1} \right)^2 \text{ and}$$

$$\sigma_{MS}^2 = \sum_{j=1}^{n_{scatt}} (R_j \Delta \Theta_j)^2 \quad (7.1)$$

The resulting design parameters are

- small r_1
- large r_2
- good space point resolution σ_1 and σ_2
- low material budget to minimize σ_{MS}^2

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