D 114600 **(Pages : 2)** **Name.....**

Reg. No.....

FIRST SEMESTER M.Sc. DEGREE (REGULAR/SUPPLEMENTARY) EXAMINATION, NOVEMBER 2024

(CBCSS)

Physics

PHY1C04—ELECTRONICS

(2019 Admission onwards)

Time : Three Hours Maximum : 30 Weightage

Section A

Answer **all** *questions.*
Each answerable in 7½ minutes.
Each question carries weightage 1.

1. Briefly explain the pinch off voltage.
2. Briefly explain biasing of FETs.
3. Define Population inversion.
4. Briefly explain different types of photodiodes.
5. Explain Open loop gain.
6. Write a short note on dominant pole.
7. Briefly explain the shift register using JK flipflop.
8. Differentiate between static and dynamic RAM

(8 × 1 = 8 weightage)

Section B

Answer any **two** *questions.*
Each question carries weightage 5.

9. Outline the construction and operation of semiconductor laser.
10. Explore closed-loop inverting op-amp configuration, deriving expressions for voltage gain, input impedance, output impedance, and bandwidth.
11. Describe the construction and working of a high-pass first order Butterworth filter. Study the frequency response. How is it converted to a second order Butterworth filter.
12. Explore the use of shift registers as counters. Discuss the concept of a ring counter and its advantages in specific applications.

(2 × 5 = 10 weightage)

Turn over

Section C

Answer any **four** *questions.*
Each question carries weightage 3.

13. With diagram and voltage truth table explain MOSFET (negative) NAND gate.
14. What is a photoconductor ? Obtain the expression for photocurrent.
15. Design a differentiator to differentiate an output signal that varies in frequency from 10 Hz to about lKHz.
16. Design a second-order low-pass filter at a high cutoff frequency of 1 kHz.
17. With the help of timing diagram and truth table explain the working of JK Master Slave flip-flop.
18. Describe the characteristic equations of D flip-flop and T flip-flop.
19. Using Karnaugh Map solve the given equation to reduce the number of gates used.

$Y = ABCD + \bar{A}BCD + A\bar{B}CD + AB\bar{C}D + ABC\bar{D}$.

(4 × 3 =12 weightage)

D 52840 **(Pages : 3)** **Name.....**

Reg. No.....

FIRST SEMESTER M.Sc. DEGREE (REGULAR/SUPPLEMENTARY) EXAMINATION, NOVEMBER 2023

(CBCSS)

Physics

PHY IC 04—ELECTRONICS

(2019 Admission onwards)

Time : Three Hours Maximum : 30 Weightage

Section A

8 *Short questions answerable within* 7.5 *minutes.*
Answer **all** *questions, each question carries weightage* 1.

1. Write a note on the frequency response of FET common source amplifier.
2. Explain quantum efficiency of an LED.
3. Draw the basic building blocks of an op-amp ?
4. List the main characteristics of an ideal Op-amp.
5. What is a flip-flop ? Give two uses.
6. Define (a) Common mode signal ; and (b) CMRR ?
7. What is Microprocessor ? List few applications of microprocessor-based system ?
8. Define slew rate.

(8 × 1 = 8 weightage)

Section B

4 *essay questions answerable within* 30 *minutes.*
Answer any **two** *questions, each question carries weightage* 5.

9. Explain the first order low and high pass filter using an op-amp and its frequency response.
10. Discuss the principle and working of a *p-n* junction solar cell. Deduce the expressions for short circuit and efficiency.

Turn over

11. Draw op-amp as a Schmidt trigger circuit and explain how a square wave generator in this circuit. What is the advantage of Schmidt trigger over zero crossing detectors ?

12. With the help of a logic diagram explain the working of a 4 bit right shift register.

(2 × 5 = 10 weightage)

Section C

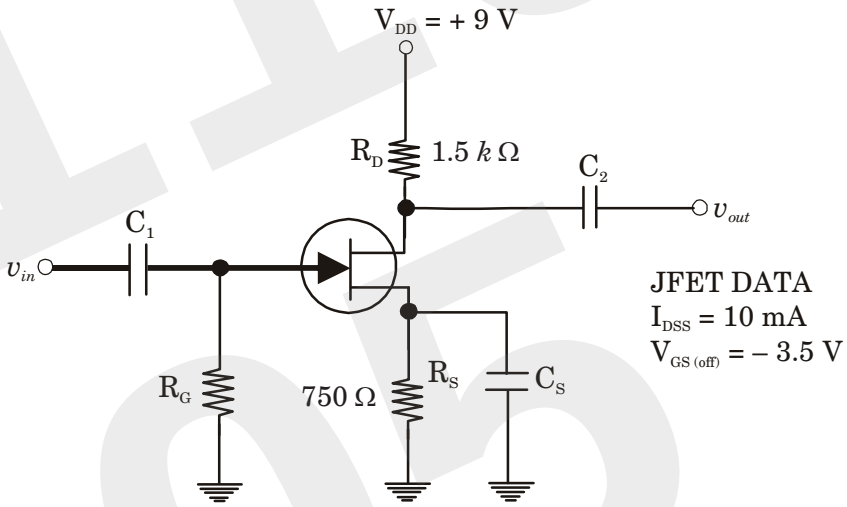
7 problems answerable within 15 minutes.
Answer any **four** *questions, each question carries weightage 3.*

13. The energy gap in a certain LED is 1.98 eV. Calculate the wavelength of the light given out. Are these radiations visible radiations ? Take $h = 6.6 \times 10^{-34}$Js.

14. How long will it take to shift an 8-bit number into a 54164 shift register if the clock is set at 10 MHz ?

15. Design a high pass filter at a cut off frequency 1 KHz (C = 0.01 μF) with pass band gain 2 and plot the frequency response.

16. For the JFET amplifier circuit shown in Figure , calculate the voltage gain with (i) RS bypassed by a capacitor ; and (ii) RS unbypassed.



17. When V_{GS} of a JFET changes from – 3.1 V to – 3 V, the drain current changes from 1 mA to 1.3 mA. What is the value of transconductance ?

18. For an op-amp used as an inverting amplifier, determine the maximum output offset voltage VI_{io}, caused by the input off set current I_{io}. Given R_F = 100 kΩ, R_1 = 1 kΩ, I_{io} = 200 μA.

19. Explain Ripple counter using logic diagram, truth table and waveform.

(4 × 3 = 12 weightage)

D 32733 **(Pages : 3)** **Name.....**

Reg. No.....

FIRST SEMESTER M.Sc. DEGREE (REGULAR/SUPPLEMENTARY) EXAMINATION, NOVEMBER 2022

(CBCSS)

Physics

PHY IC 04—ELECTRONICS

(2019 Admission onwards)

Time : Three Hours Maximum : 30 Weightage

Section A

Answer **all** *questions.*
Each question carries weightage 1.

1. What is unity-gain bandwidth of an operational amplifier ?
2. How can you change the frequency of emission in a LED ? Give any *two* examples for different colours.
3. Briefly explain radiative transition in a tunnel diode.
4. Write any *two* differences between common source and common drain operations of FET.
5. Briefly explain the advantages of Karnaugh map in logic circuit design.
6. Distinguish between microprocessor and Microcomputer.
7. Write a short note on population inversion.
8. How can you convert an SR Flip-flop to a JK Flip-flop ?

(8 × 1 = 8 weightage)

Section B

Answer any **two** *questions.*
Each question carries weightage 5.

9. With the help of a logic diagram explain the working of a ring counter.
10. How can you construct an active low pass filter using operational amplifier ? Explain its working.

Turn over

11. Explain the different biasing techniques used in JFET and also explain the working of a common Source amplifier.

12. With the help of an R - 2R network circuit explain the conversion of a 4 bit digital signal to analog signal.

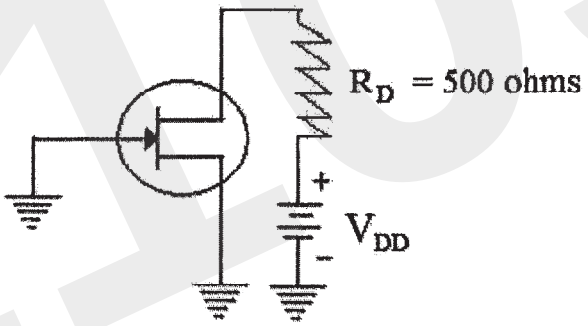
(2 × 5 = 10 weightage)

Section C

Answer any **four** *questions.*
Each question carries weightage 3.

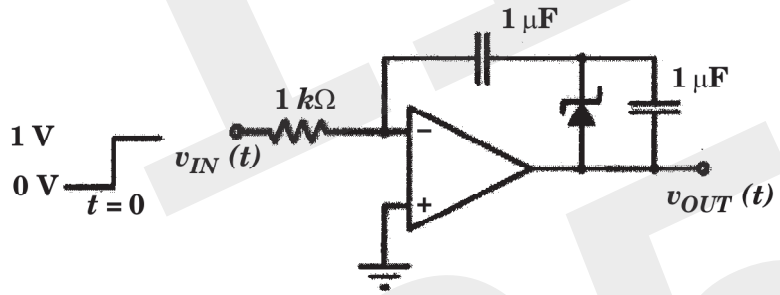
13. Show how an asynchronous counter can be implemented having a modulus of 12 with a straight binary sequence from 0000 through 1011.

14. For the JFET in the given figure, $V_{GS\ (off)}$ is – 3 V and I_{DSS} is 10 mA. Determine the minimum value of V_{DD} required to put the device in constant current area of operation.



15. Design a practical differentiator that will differentiate signals with frequencies up to 400 Hz. The gain at 10 Hz should be 0.12. If the op amp used in the design has a unity gain frequency of 2 MHz, what is the upper cutoff frequency of the differentiator ?

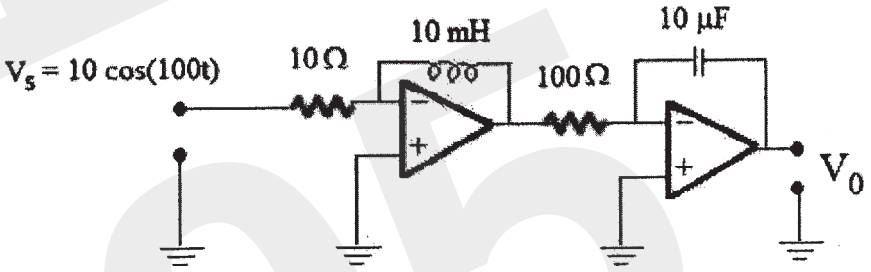
16. In the circuit shown below, the op-amp is ideal and Zener voltage of the diode is 2.5 volts. At the input, unit step voltage is applied, i.e. $v_{IN}(t) = u(t)$ volts. Also, at $t = 0$, the voltage across each of the capacitors is zero. Find the time 't' in milliseconds, at which the output voltage v_{OUT} crosses the Zener break down.



17. Using Karnaugh Map solve the given equation to reduce the number of gates used.

$Y - ABCD \mid \bar{A}BCD \mid AB\bar{C}D \mid AB\overline{CD}$.

18. In the figure given below assume the ideal op amp is used. Find the output voltage if an input signal Vs = 10 cos(100t) is applied.



19. Draw the logical circuit of an synchronous decade counter.

(4 × 3 = 12 weightage)

D 13160 **(Pages : 3)** **Name.....**

Reg. No.....

FIRST SEMESTER M.Sc. DEGREE (REGULAR/SUPPLEMENTARY) EXAMINATION, NOVEMBER 2021

(CBCSS)

Physics

PHY 1C 04—ELECTRONICS

(2019 Admission onwards)

Time : Three Hours Maximum : 30 Weightage

General Instructions

1. *In cases where choices are provided, students can attend* **all** *questions in each section.*
2. *The minimum number of questions to be attended from the Section / Part shall remain the same.*
3. *The instruction if any, to attend a minimum number of questions from each sub section / sub part / sub division may be ignored.*
4. *There will be an overall ceiling for each Section / Part that is equivalent to the maximum weightage of the Section / Part.*

Section A

8 *Short questions answerable within* 7½ *minutes.*
Answer **all** *questions, each carry weightage* 1.

1. How is digital switching done using MOSFET ?
2. Give the basic principle of the working of Light dependent resistor (LDR). Mention its application.
3. Define the term CMRR and explain what will be the condition for CMMR to infinite.
4. Differentiate between wide band reject filter and narrow band reject filter.
5. What are ripple counters ? Give its advantages.
6. Give the principle of working of an IR emitter. Mention two uses.
7. What are the functions of an accumulator ?
8. Give two characteristics of a non-inverting amplifier.

(8 × 1 = 8 weightage)

Turn over

Section B

4 essay questions answerable within 30 minutes.

Answer any **two** *questions, each carry weightage 5.*

9. Explain the working of MOSFET under depletion mode. Also explain the working of enhancement type MOSFET.

10. Explain the construction and operation of semiconductor lasers.

11. What are Butterworth filters ? Explain the design and working of a first order low-pass and high pass filters using op-amp.

12. Explain the internal architecture of 8085 microprocessor.

(2 × 5 = 10 weightage)

Section C

7 problems answerable within 15 minutes.

Answer any **four** *questions, each carry weightage 3.*

13. For a light emitting diode made of GaAsP, the energy gap is 1.90 eV. What is the wavelength of radiations emitted ? Are these radiations visible radiations ? Take $h = 6.6 \times 10^{-34}$ Js.

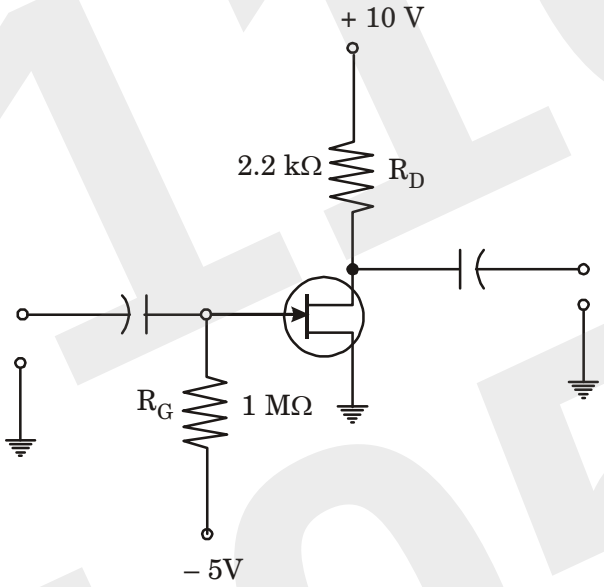
14. Explain narrow band-pass filter. Design a narrow band-pass filter so that

    $f_c = 1$ kHz, $Q = 3$, $A_F = 10$.

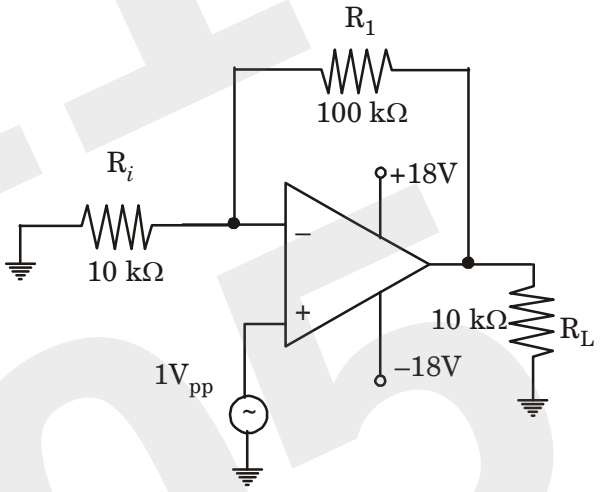
15. A power amplifier has a power gain of 40 db. If an input power of 3 mW is applied, then calculate the output power.

16. Design a second order low-pass filter for a cut-off frequency 1 kHz (C = 0.01 μF).

17. JFET in given Figure has values of $V_{GS\ (off)} = -8V$ and $I_{DSS} = 16$ mA. Determine the values of V_{GS}, I_D and V_{DS} for the circuit :



18. For the noninverting amplifier circuit shown in Figure, find (i) Closed loop voltage gain ; and (ii) Maximum operating frequency. The slew rate is 0.5 V/μs.



19. Describe master slave JK flip-flop.

(4 × 3 = 12 weightage)

2087

D 93435 (Pages : 3) Name.....

Reg. No.....

FIRST SEMESTER M.Sc. DEGREE (REGULAR/SUPPLEMENTARY) EXAMINATION, NOVEMBER 2020

(CBCSS)

Physics

PHY IC 04—ELECTRONICS

(2019 Admissions)

Time : Three Hours Maximum : 30 Weightage

General Instructions

1. *In cases where choices are provided, students can attend* **all** *questions in each section.*
2. *The minimum number of questions to be attended from the Section / Part shall remain the same.*
3. *There will be an overall ceiling for each Section / Part that is equivalent to the maximum weightage of the Section / Part.*

Section A

Answer **all** *questions, each carries weightage* 1.

1. Briefly explain any *two* ideal parameters of an operational amplifier.
2. How can you change the colours of emission in a LED ? Give any *two* examples for different colours.
3. Briefly explain fill factor and efficiency.
4. Distinguish between BJT and FET.
5. Briefly explain the advantages of Karnaugh map in logic circuit design..
6. Describe the working of a PN junction diode as a solar cell.
7. Write a short note on switching action of a MOSFET.
8. How can you convert an SR Flip-flop to a D Flip-flop ?

(8 × 1 = 8 weightage)

Section B

Answer any **two** *questions, each carries weightage* 5.

9. With the help of a logic circuit briefly explain the working of a decade counter.
10. How can you construct an active high pass filter using operational amplifier ? Explain its working.

Turn over

11. What is the use of positive feedback ? With the help of a circuit explain the working of a Wien bridge oscillator.

12. With the help of a circuit explain the conversion of an analog signal to digital signal.

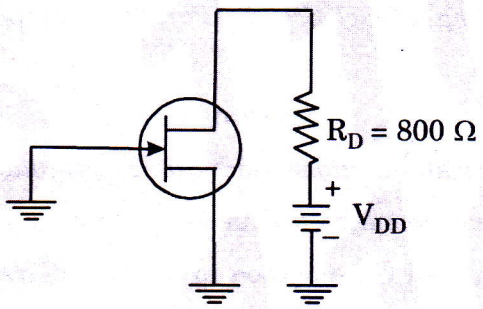
(2 × 5 = 10 weightage)

Section C

Answer any **four** *questions, each question carries weightage* 3.

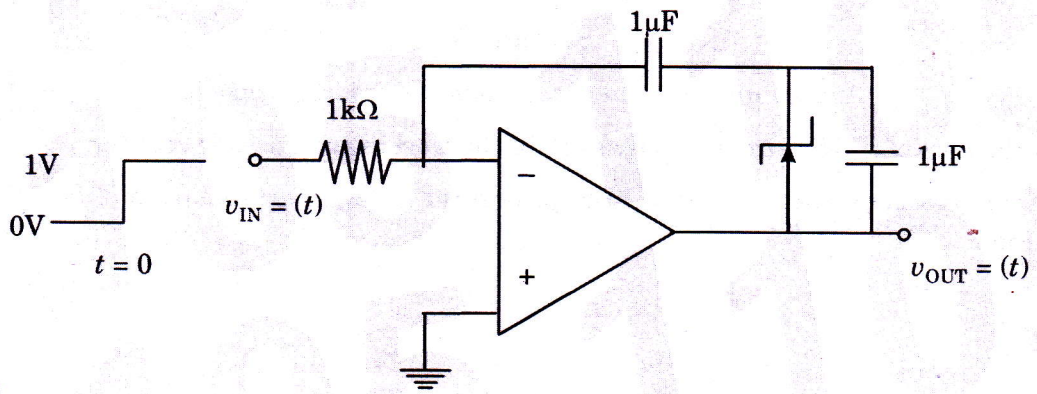
13. Design an Integrator that integrates signals with frequencies down to 200 Hz and produces a peak output of 0.5 V when the input used is a 25 V peak sine wave having frequency 20 kHz.

14. For the JFET in the given figure, $V_{GS\ (off)}$ is –4V and I_{DSS} is 10 mA. Determine the minimum value of V_{DD} required to put the device in constant current area of operation :



15. Design a first order Butterworth low pass filter circuit using operational amplifier with a cutoff frequency 15.9 kHz. C = 0.001 μ F and A_{max} = 1.5

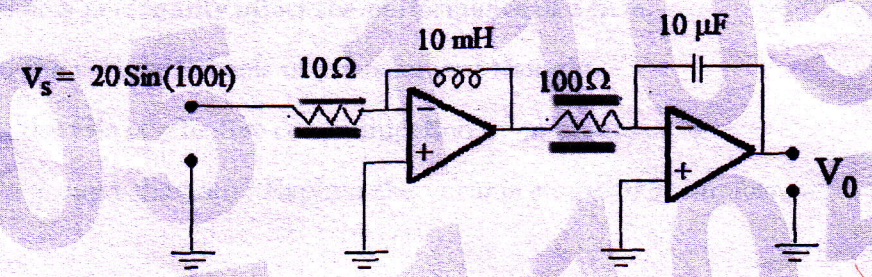
16. In the circuit shown below, the op-amp is ideal and Zener voltage of the diode is 2.5 volts. At the input, unit step voltage is applied, *i.e. vin* (*t*) = *u* (*t*) volts. Also, at *t* = 0, the voltage across each of the capacitors is zero. Find the time '*t*' in milliseconds, at which the output voltage V_{out} crosses the Zener break down.



17. Using Karnaugh Map solve the given equation to reduce the number of gates used :

$$Y = \bar{A}\bar{B}CD + \bar{A}BCD + ABCD + A\bar{B}CD + AB\bar{C}\bar{D} + AB\bar{C}D + ABC\bar{D}.$$

18. In the figure given below assume the ideal op-amp is used. Find the output voltage if an input signal $V_s = 20 \text{ Sin } (100t)$ is applied.



19. Design an astable multi-vibrator using operational amplifier to get 500 Hz.

(4 × 3 = 12 weightage)

D 72798 (Pages : 2) Name.....

Reg. No.....

FIRST SEMESTER M.Sc. DEGREE EXAMINATION, DECEMBER 2019

(CUCSS)

Physics

PHY1C04—ELECTRONICS

(2017 Admissions)

Time : Three Hours Maximum : 36 Weightage

Section A

Answer **all** *questions.*
Each question carries weightage 1.

1. Give a short note on Complementary MOSFET (CMOS) arrangement.
2. Explain the operation of FET as a Voltage-Variable Resistor (VVR) ?
3. Explain the working of a Tunnel diode with its static current-voltage characteristics.
4. What are intrinsic and extrinsic transitions in a semiconductor ? Derive an expression for photon flux.
5. What is a photodiode ? Give a short note on different types of photodiodes.
6. Explain slew rate.
7. What do you mean by frequency scaling ?
8. Define input offset current.
9. Differentiate JK and RS flip-flops.
10. Write any two data transfer instructions and explain it.
11. Explain the function of ALU in 8085.
12. What do you mean by band reject filter ?

(12 × 1 = 12 weightage)

Section B

Answer any **two** *questions.*
Each question carries weightage 6.

13. Explain Metal Qxide-Semiconductor FET (MOSFET). Differentiate Enhancement and Depletion layer MOSFETs.
14. Explain how an op-amp can be used as differentiator with neat diagram and deduce the expression for output voltage.

Turn over

15. Explain the first order low and high-pass filter using an op-amp and its frequency response.
16. Explain the internal architecture of 8085 microprocessor.

(2 × 6 = 12 weightage)

Section C

Answer any **four** *questions.*
Each question carries weightage 3.

17. Calculate the confinement factor for a GaAs laser with an active region thickness 1 μm, refractive index 3.6, and critical angle at the active-to-nonactive boundary of 84°. Assume the C constant to be $8 \times 107\ m^{-1}$.
18. A MOSFET has a drain-circuit resistance R_d of 100 K and operates at 20 kHz. Calculate the voltage gain of this device as a single stage, and then as the first transistor in a cascaded amplifier consisting of two identical stages. The MOSFET parameters are g_m = 1.6 mA/V, r_d = 44 K, C_{gs} = 3.0pF, C_{ds} = 1.0 pF, and C_{gd} = 2.8 pF.
19. Deduce the common mode and differential gain equations of an emitter coupled differential amplifier.
20. Describe the working of master slave JK flip-flop
21. Design a high pass filter at a cutoff frequency of 1 KHz with a pass band gain of 2 and plot the frequence response.
22. Explain the wide and narrow band pass filters.

(4 × 3 = 12 weightage)

D 72981 (Pages : 2) Name.....

Reg. No.....

FIRST SEMESTER M.A./M.Sc./M.Com. DEGREE EXAMINATION DECEMBER 2019

(CBCSS)

Physics

PHY 1C 04—ELECTRONICS

(2019 Admissions)

Time : Three Hours Maximum : 30 Weightage

Section A

Answer **all** *questions.*
Each question carries weightage 1.

1. What is Multi-vibrator ? Classify them.
2. Write all the four different types of filters ?
3. Briefly explain zener and avalanche breakdowns.
4. Explain 3 dB cutoff frequency ? Why is it 3 dB, not 1 dB ?
5. What is Positive logic and Negative Logic ?
6. Obtain the expression for loop gain of an inverting amplifier using Op-amp.
7. Write a short note on LDR.
8. How can you convert a JK Flip-flop to a Register ?

(8 × 1 = 8 weightage)

Section B

Answer any **two** *questions.*
Each question carries weightage 5.

9. With the help of a logic diagram explain the working of a 4 bit right shift register.
10. Explain the working of a second order low pass and high pass Butterworth filter with the help of circuit diagram.
11. Explain the different biasing techniques used in JFET and also explain the working of a common drain amplifier.
12. Give the structure and operation of depletion MOSFET. How is depletion MOSFET different from enhancement MOSFET ? With the help of a circuit explain the working of a NOT Gate.

(2 × 5 = 10 weightage)

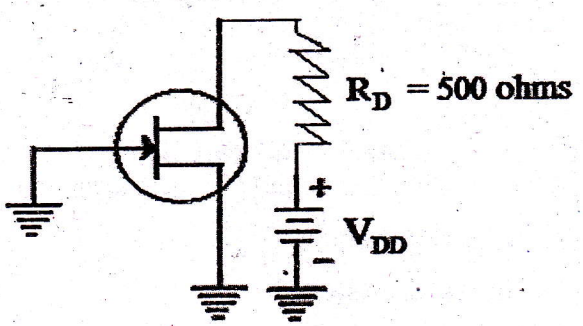
Turn over

Section C

Answer any **four** *questions.*
Each question carries weightage 3.

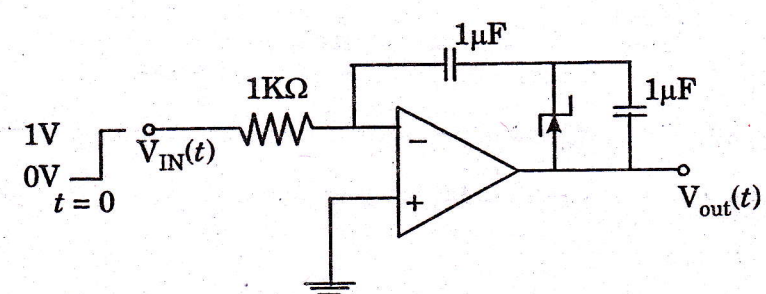
13. Show how an asynchronous counter can be implemented having a modulus of 9 with a straight binary sequence from 0000 through 1000.

14. For the JFET in the given figure, $V_{GS(off)}$ is – 6V and I_{DSS} is 15 mA. Determine the minimum value of V_{DD} required to put the device in constant current area of operation.



15. Design a practical differentiator that will differentiate signals with frequencies up to 400 Hz. The gain at 10 Hz should be 0.12. If the op-amp used in the design has a unity gain frequency of 2 MHz, what is the upper cutoff frequency of the differentiator ?

16. In the circuit shown below, the op-amp is ideal and Zener voltage of the diode is 2.5 volts. At the input, unit step voltage is applied, i.e. $V_{IN}(t) = u(t)$ volts. Also, at $t = 0$, the voltage across each of the capacitors is zero. Find the time 't' in milliseconds, at which the output voltage V_{OUT} crosses the Zener break down.



17. Using Karnaugh Map solve the given equation to reduce the number of gates used.

$$Y = ABCD + \bar{A}BCD + AB\bar{C}D + AB\bar{C}\bar{D}.$$

18. In the figure given below assume the ideal op amp is used. Find the output voltage if an input signal Vs = 15 cos (50t) is applied.

19. Draw the logical circuit of an synchronous decade counter.

(4 × 3 = 12 weightage)

D 51455 (Pages : 2) Name.....

Reg. No.....

FIRST SEMESTER M.Sc. DEGREE EXAMINATION, NOVEMBER 2018

(CUCSS—PG)

Physics

PHY 1C 04—ELECTRONICS

(2017 Syllabus Year)

Time : Three Hours Maximum : 36 Weightage

Section A

Answer **all** *questions.*

Each question carries weightage 1.

1. Define the threshold voltage of MOSFET.
2. Draw the circuit diagram of CMOS inverter, and explain its operation.
3. Explain the working of a tunnel diode.
4. Differentiate between visible and IR LEDs.
5. Explain the working of p-n junction solar cell.
6. What are the characteristics of an ideal operational amplifier ?
7. What is CMRR? What is its importance ?
8. Explain the action of a voltage follower.
9. What are the advantages of active filters over passive filters ?
10. Distinguish between dynamic and static RAM.
11. Explain the operation of JK flipflop.
12. Briefly explain the working of a ring counter.

(12 × 1 = 12 weightage)

Section B

Answer any **two** *questions.*

Each question carries weightage 6.

13. Explain the construction and working of N-channel JFET. Discuss the static and transfer characteristics. Obtain the expressions for drain resistance, amplification factor and transconductance.

Turn over

14. Explain the construction and operation of semiconductor laser.

15. Discuss the working of an emitter coupled differential amplifier and hence obtain the expressions for common mode and differential gain.

16. With the help of a block diagram explain the architecture of 8085 microprocessor.

(2 × 6 = 12 weightage)

Section C

Answer any **four** *questions.*
Each question carries weightage 3.

17. Sketch the cross section of an n-channel enhancement MOSFET.Draw the drain characteristics and the transfer curve.

18. What is a photoconductor ? Obtain the expression for photocurrent.

19. For an op amp used as an inverting amplifier, determine the maximum output offset voltage VI_{io}, caused by the input offset current I_{io}. Given $R_F = 100\ K\Omega$, $R_1 = 1\ K\Omega$, $I_{io} = 200nA$.

20. The input to the differentiator circuit is a sinusoidal voltage of peak value 5mV and frequency 1KHz. Find the output if $R = 100\ K\Omega$ and $C = 1\mu F$.

21. Design a low pass filter at a cut off frequency of 1kHz with a pass band gain of 2.

22. $F = \bar{A}C + \bar{A}B + A\bar{B}C + BC$ is a logic equation. Make truth table and simplify using K map.

(4 × 3 = 12 weightage)

C 32347 (Pages : 2) Name.....

Reg. No.....

FIRST SEMESTER M.Sc. DEGREE EXAMINATION, DECEMBER 2017

(CUCSS)

Physics

PHY 1C 04—ELECTRONICS

(2017 Admissions)

Time : Three Hours Maximum : 36 Weightage

Section A

Answer **all** *questions.*
Each carries weightage of 1.

1. Define the pinch off voltage.
2. Explain the operation of FET as VVR.
3. Draw the V-I characteristics of a tunnel diode and explain each region.
4. Briefly explain the working of semiconductor laser.
5. What are the three methods of compensations ?
6. Explain why open loop op amp configurations are not used in linear applications.
7. Define slew rate and unity gain bandwidth.
8. Explain the working of summing circuit using inverting op amp configuration.
9. What is a Schmidt trigger ?
10. Explain the operation of MSJK flip-flop.
11. Distinguish between synchronous and asynchronous counters.
12. Discuss the register organization of 8085 microprocessor.

(12 × 1 = 12 weightage)

Turn over

Section B

Answer any **two** *questions.*
Each carries weightage 6.

13. Discuss the principle and working of a pn junction solar cell. Deduce the expressions for short circuit current and efficiency.

14. Discuss the closed loop inverting op amp configuration and get the expressions for voltage gain, input impedance, output impedance and bandwidth.

15. What are Butterworth filters ? Explain the design and working of a first order low pass and high pass filters using op amp.

16. What is meant by D/A converter ? Discuss the R-2R ladder D/A converter.

(2 × 6 = 12 weightage)

Section C

Answer **four** *questions.*
Each carries weightage 3.

17. Obtain the expressions for the voltage gain of common source and common drain FET amplifiers at high frequencies.

18. Explain with the help of a diagram, any two biasing techniques used in FET amplifier circuits.

19. If the photon output of a laser diode is equal to the band gap energy, find the wavelength separation between adjacent resonant modes in GaAs laser with L = 75μm.

20. Consider a non-inverting amplifier with $R_l = 1\ k\Omega$, $R_F = 10\ k\Omega$ and $R_i = 2\ M\Omega$, $R_o = 75\ \Omega$, $f_o = 5Hz$. Determine A_F, R_{iF}, R_{oF} and f_F of the amplifier.

21. Design a differentiator to differentiate an input signal that varies in frequency from 10 Hz to about 1 kHz.

22. Simplify the Boolean expression $F = AB + \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C}$ using Karnaugh map.

(4 × 3 = 12 weightage)

C 32343 (Pages : 2) Name.....

Reg. No.....

FIRST SEMESTER M.Sc. DEGREE EXAMINATION, DECEMBER 2017

(CUCSS)

Physics

PHY 1C 04—ELECTRONICS

(2012 Admissions)

Time : Three Hours Maximum : 36 Weightage

Section A

Answer **all** *questions.*

Each question carries a weightage of 1.

1. What is drain resistance ? Give the relation between drain resistance and drain current.
2. Draw the volt-ampere drain characteristics of a P-channel E-MOSFET.
3. What is the basic principle of the working of LDR ? Mention its application:-
4. Write the relation between light intensity in a semiconductor and absorption coefficient. What is its significance ?
5. What are the characteristics of an ideal op amp ?
6. What is the slew rate of an op amp ? Write the relation between maximum frequency of the signal voltage and slew rate.
7. Why Schmitt trigger is preferred to zero crossing detector ?
8. Explain the functions of ALE and IO/$\overline{m}$ signals of the 8085 microprocessor.
9. Write the description of the following instructions : INR C, JM 3000H, JMP 2085H, OUT 01H.
10. Compare C MOS with TTL.
11. The FF is essentially a 1-bit memory. Why ?
12. In analogue computers, integrators are preferred to differentiators. Why ?

(12 × 1 = 12 weightage)

Turn over

Section B

Answer any **two** *questions.*
Each question carries a weightage of 6.

13. Explain the working of MOSFET under depletion mode. Also explain the working of enhancement type MOSFET

14. What is a tunnel diode ? Explain the principle of working of a tunnel diode, giving its characteristics.

15. Explain how a square wave is generated in an op amp based square wave generator.

16. What is a ripple counter ? Why is it called so ? How many FF s would be needed to count the number 7 ? Explain its working.

(2 × 6 = 12 weightage)

Section C

Answer any **four** *questions.*
Each carries a weightage of 3.

17. When V_{GS} of a FET changes from –3.1 V to 3 V, the drain current changes from 1mA to 1.3mA ? Find the value of transconductance.

18. A photodiode has a quantum efficiency of 65% when photons of energy 1.5×10^{-19} J are incident upon it. At what wavelength is the photodiode operating ?

19. What is the error in the differential output, if the inputs V_1 = 1050 μV, V2 = 950μ Vand CMRR = 1000 ?

20. Design a high pass filter for a cut-off frequency of 2 kHz and pass band gain 2.

21. The inverting and non-inverting terminals of an opamp are grounded. If the op amp has an input offset voltage of 5mV and an open loop voltage gain of 10,000, then what will be the output voltage ?

22. Write an assembly language programme for adding the contents of the memory location 8000H and 8050H. Store the result in 8100H.

(4 × 3 = 12 weightage)

D 3196 (Pages : 2) Name.....

Reg. No.....

FIRST SEMESTER M.Sc. DEGREE EXAMINATION, DECEMBER 2016

(CUCSS)

Physics

PHY 1C 04—ELECTRONICS

(2012 Admissions)

Time : Three Hours Maximum : 36 Weightage

Section A

Answer **all** *questions.*
Each question carries a weightage of 1.

1. What is drain conductance ? Give the relation between drain conductance and drain current.
2. Why are the MOSFET circuits slower than the corresponding bipolar circuits ?
3. Draw the Schematic diagram of a simplified pn junction photodiode.
4. What is the basic principle of working of LDR ? Mention its application.
5. What are the advantages of integrators over differentiators in practical applications ?
6. Which are the externally initiated interrupt signals of 8085 microprocessor ? Write its priority order.
7. The FF is essentially a 1-bit memory or storage unit. Why ?
8. What is propagation delay time ? How it is related with the solution of racing problem in flip-flops ?
9. How does the voltage follower prevent the loading effect in a circuit ?
10. JMP 3000H and JM 4000H are branch group of instructions. What is the difference between the two ?
11. Compare CMOS with TTL.
12. Explain the instructions of 8085 microprocessor :
    (a) LXI B 6000H.
    (b) LDA 6500H.

(12 × 1 = 12 weightage)

Turn over

Section B

Answer any **two** *questions.*
Each question carries a weightage of 6.

13. Sketch the circuit of a common source amplifier : Derive the expression for the voltage gain at low frequencies. What is the maximum value of A_v ? Compare the common source stage with the common drain configuration.

14. With the help of Schematic diagram of a typical solar cell, explain its working principle.

15. Draw a Schmitt trigger circuit and explain how a square wave generator in this circuit. What is the advantage of Schmitt trigger over zero crossing detectors?

16. Explain the working of a 3-bit ripple counter using JK FF. Also draw its timing diagram?

(2 × 6 = 12 weightage)

Section C

Answer any **four** *questions.*
Each question carries a weightage of 3.

17. Keeping the gate-voltage constant, the drain to source voltage of a FET is changed from 15 V to 5 V. The drain current then changes by 100μmA. Calculate the drain resistance of the FET.

18. The band gap of GaAs LED at 300k is 1.42 eV, which changes (decreases) with temperature as $\frac{dE_g}{dT} = -4.4 \times 10^{-4}$ eV/K. What is the change in the emitted wavelength, if the temperature change is 10°C ?

19. A schimit trigger is found to switch on due to the application of 2.65 V as the input, but it is formed to switch of only at 1.9 V :
    (a) What is the hysteresis voltage of the schimit trigger ?
    (b) What is the minimum amplitude of the input signal that will produce an output ?

20. Design a low-pass filter for a cut-off frequency of 2 kHz and pass band gain 2.

21. Explain the working of an opamp as scale changer.

22. Write an assembly language programme for adding the contents of memory location 8000H and 8050H. Store the result in 8100 H.

(4 × 3 = 12 weightage)

D 92958 (Pages : 2) Name.....

Reg. No.....

FIRST SEMESTER M.Sc. DEGREE EXAMINATION, DECEMBER 2015

(CUCSS)

Physics

PHY 1C 04—ELECTRONICS

(2012 Admission onwards)

Time : Three Hours Maximum : 36 Weightage

Part A

Answer **all** *questions.*
Each question carries 1 *weightage.*

1. What is transconductance ? Give the relation between transconductance and gate source cut-off voltage.
2. Briefly explain the working of E-MOSFET.
3. Explain how the negative resistance region of a tunnel diode is used in the design of tunnel diodes.
4. Give the basic principle of the working of LDR. Mention its application.
5. What is an IR emitter ? How does it work ?
6. Define : (a) Common mode signal ; (b) Difference mode signal ; (c) CMRR ; (d) What is the value of CMRR for an ideal op-amp ?
7. Give *two* characteristics of a non-inverting amplifier.
8. Draw the circuit of an op-amp as a scale changer.
9. What is a clocked flip-flop ? Name *two* inputs of a clocked flip-flop.
10. What are ripple counters ? Give its disadvantages.
11. Compare CMOS with TTL.
12. What is a zero crossing detector ?

(12 × 1 = 12 weightage)

Part B

Answer any **two** *questions.*
Each question carries 6 *weightage.*

1. Draw the circuit of a common source amplifier with load resistor R_d in the drain circuit and an additional resistor R_s in the source to ground circuit. Draw the Thevenin's equivalent circuit looking into the drain. Derive the expressions for voltage gain and output resistance.

Turn over

2. Explain the principle of working of a semiconductor laser. How is population inversion achieved in a semiconductor ? Describe the construction and working of a PN Junction Laser.
3. Discuss the Dominant Pole Compensation method. What are the merits and demerits of this method?
4. Explain the operation of a JK flip-flop. Give its truth table. What is a race around condition of a JK flip-flop ? How is it eliminated in master slave JK flip-flop ?

(2 × 6 = 12 weightage)

Part C

Answer any **four** *questions.*
Each question carries **3** *weightage.*

1. A solar cell is realized in a semiconductor having bandgap of 1.3 V. Estimate the maximum possible short circuit current of the cell for AM 1.5 spectrum.
2. Determine the energy in eV associated with photons of green light of wavelength 5000 Å.
3. Design a low-pass filter for a cut-off frequency of 2 kHz and pass band gain of 2.
4. Explain the working of an op-amp as a summing amplifier.
5. Expand A (B + A) B to maxterms and min terms.
6. Draw the circuit diagram equivalent circuits and truth table of the NMOS gate.

(4 × 3 = 12 weightage)

D 72897 (Pages : 2) Name.....

Reg. No.....

FIRST SEMESTER M.Sc. DEGREE EXAMINATION, DECEMBER 2014

(CUCSS)

Physics

PHY 1C 04—ELECTRONICS

(2012 Admission onwards)

Time : Three Hours Maximum : 36 Weightage

Part A

Answer **all** *questions.*
Each question carries 1 *weightage.*

1. What is transconductance ? Give the relation between transconductance and gate source cutoff voltage.
2. How is Digital switching done using MOSFET ?
3. What are the essential differences between a tunnel diode and a semiconductor junction diode?
4. Give the basic principle of the working of LDR. Mention its application.
5. Give the principle of working of an IR emitter. Mention two uses.
6. List the main characteristics of an ideal op-amp.
7. Give two characteristics of a non-inverting amplifier.
8. Draw the circuit of an op-amp as an adder.
9. What is a flip-flop ? Give two uses.
10. What are ripple counters ? Give its disadvantages.
11. What are the merits of CMOS ? Where are they used ?
12. Distinguish between active filters and Passive filters.

(12 × 1 = 12 weightage)

Part B

Answer any **two** *questions.*
Each question carries 6 *weightage.*

1. With the help of a circuit describe the working og a JFET common source amplifier. Derive expressions for the DC drain current I_D and DC drain voltage V_D.
2. Describe the construction and working of an emitter coupled differential amplifier. What are its limitations ? Explain why CMMR $\rightarrow \infty$ for a symmetrical circuit.

Turn over

3. Describe the operation of a Schmitt trigger. Draw its transfer characteristic. How is a slow varying input voltage converted into an output voltage having abruptly varying wave forms using a Schmitt Trigger.

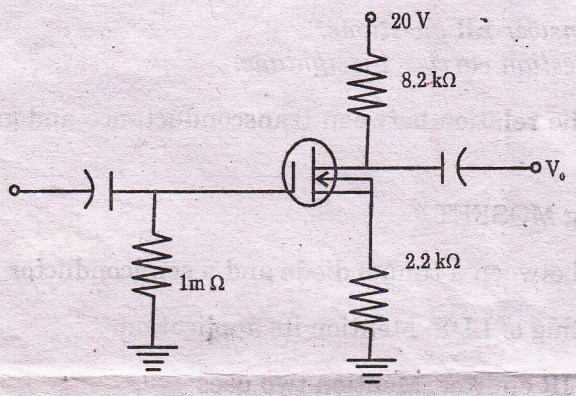
4. Explain CMOS Logic. Discuss the working of (a) CMOS Inverter ; (b) CMOS NAND Gate.

(2 × 6 =12 weightage)

Part C

Answer any **four** *questions.*
Each question carries 3 *weightage.*

1.



If ID_{SS} = 8mA, Vp = – 8V Determine I_{DQ} and V_{GSQ} and V_D (Q is operating point)

2. A solar cell is realized in a material with the band gap of 1.3eV. What will happen to its efficiency if its temperature is increased by 40 % ?

3. Determine the output voltage of an op-amp integrator when a 5mV, 1KHz sinusoidal signal is applied (R = 100K, C = 1μF).

4. Draw the circuit of a square wave generator using op-amp. Obtain the equation for frequency oscillation.

5. Explain how an active resonant band pass filter is constructed using op-amp. What is its characteristics ?

6. Explain the working of a static RAM. Where are they used ?

(4 × 3 = 12 weightage)

D 52983 (Pages : 2) Name.....

Reg. No.....

FIRST SEMESTER M.Sc. DEGREE EXAMINATION, JANUARY 2014

(CUCSS)

PHY IC 04—ELECTRONICS

(2012 Admissions)

Time : Three Hours Maximum : 36 Weightage

Part A

Answer **all** *questions.*
Each question carries 1 *weightage.*

1. What is transconductance ? Give the relation between transconductance and gate source cutoff voltage.
2. Briefly explain the working of D-MOSFET.
3. Explain how the negative resistance region of a tunnel diode is used in the design of tunnel diodes.
4. Give the basic principle of the working of LDR. Mention its application.
5. Explain the term 'Dark Current' in relation to a Photodiode.
6. Define :
   (a) Common mode signal.
   (b) Difference mode signal.
   (c) CMRR.
   (d) What is the value of CMRR for an ideal op-amp ?
7. Give two characteristics of a non-inverting amplifier.
8. Draw the circuit of an op-amp as a sign changer.
9. What is a clocked flip-flop ? Name two inputs of a clocked flip-flop.
10. What are ripple counters ? Give its disadvantages.
11. Why is the fan out of CMOS very high ?
12. What is a zero crossing detector ?

(12 × 1 = 12 weightage)

Turn over

Part B

Answer any **two** *questions.*
Each question carries 6 *weightage.*

1. Draw the circuit of a common drain amplifier with a load resistor R_s in the chain to ground circuit and an additional resistor R_d in the drain circuit. Draw the Thevenin's equivalent circuit looking into the drain. Derive expressions for the voltage gain and output resistance.
2. Describe the basic requirements for solar cell design. What are the different losses in solar cells ? Enlist them.
3. Describe the construction and working of a high-pass first order Butterworth filter. Study the frequency response. How is it converted to a second order Butterworth filter.
4. What are the procedures followed in the Design of Synchronous counters. Design a Synchronous 3 bit up-down counter using J-K FFS.

(2 × 6 = 12 weightage)

Part C

Answer any **four** *questions.*
Each question carries 3 *weightage.*

1. Given I_{DSS} = 6 mA and V_p = –4.5 V, Determine I_D at V_{GS} = –2 V and –3.6 V and determine VGS at I_D = 3 mA and 5.5 mA.
2. A solar cell has an open circuit voltage of 630 mV. What would be its FF ? What is the approximate value of FF for a good solar cell ?
3. Explain the principle of working of a Photodiode. Draw the Photodiode characteristics and explain.
4. Design a second order low-pass filter for a cut-off frequency of 1kHz $(C = 0.01 - \mu F)$.
5. Explain the working of an op-amp as a V to I converter.
6. Expand $A(A + B)(A + B + C)$ to max terms and min terms.

(4 × 3 = 12 weightage)